X67DM1321.L12(-1)

1 General information

This module has 16 digital channels that can be configured as inputs or outputs. The inputs are designed for sink connections, the outputs for source connections.

- 16 digital channels, configurable as inputs or outputs
- Replacement of passive distributors
- 2 additional channels with counter functions
- All outputs with single-channel diagnostics
- Extensive additional status information

2 Order data

Model number	Short description	Figure
	Digital mixed modules	
X67DM1321.L12	X67 digital mixed module, 16 channels configurable as inputs or outputs, 24 VDC, 0.5 A, configurable input filter, 2 event counters 50 kHz, M12 connectors, high-density module	
X67DM1321.L12-1	X67 digital mixed module, 16 channels configurable as input or output, 24 VDC, 0.5 A, pinning variant, configurable input filter, 2 event counters 50 kHz, M12 connectors, high-density module	

Table 1: X67DM1321.L12, X67DM1321.L12-1 - Order data

Required accessories
For a general overview, see section "Accessories - General overview" of the X67 system user's manual.

3 Technical data

Model number	X67DM1321.L12	X67DM1321.L12-1
Short description		
I/O module	16 digital channels, configurable as inputs or outputs using software, inputs with additional functions	
General information		
Isolation voltage between channel and bus	500 V_{Eff}	
Nominal voltage	24 VDC	
B&R ID code	0x1A1D	0xDAC0
Sensor/Actuator power supply	0.5 A summation current	
Status indicators	I/O function for each channel, supply voltage, bus function	
Diagnostics		
Outputs	Yes, using status LED and software	
I/O power supply	Yes, using status LED and software	
Connection type		
X2X Link	M12, B-keyed	
Inputs/Outputs	8x M12, A-keyed	
I/O power supply	M8, 4-pin	
Power consumption		
Internal I/O	3 W	
X2X Link power supply	0.75 W	
Certifications		
CE	Yes	
KC	Yes	-
EAC	Yes	
UL	cULus E115267 Industrial control equipment	
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5	
ATEX	Zone 2, II 3G Ex nA IIA T5 Gc IP67, Ta = 0 - Max. 60°C TÜV 05 ATEX 7201X	
I/O power supply		
Nominal voltage	24 VDC	
Voltage range	18 to 30 VDC	
Integrated protection	Reverse polarity protection	
Power consumption		
Sensor/Actuator power supply	Max. 12 W [1)]	
Sensor/Actuator power supply		
Voltage	I/O power supply minus voltage drop for short circuit protection	
Voltage drop for short-circuit protection at 0.5 A	Max. 2 VDC	
Summation current	Max. 0.5 A	
Short-circuit proof	Yes	
Digital inputs		
Input voltage	18 to 30 VDC	
Input current at 24 VDC	Typ. 4.4 mA	
Input characteristics per EN 61131-2	Type 1	
Input filter		
Hardware	≤10 µs (channels 1 to 4) / ≤70 µs (channels 5 to 16)	
Software	Default 0 ms, configurable between 0 and 25 ms in 0.2 ms intervals	
Input circuit	Sink	
Additional functions	50 kHz event counting, gate measurement	
Input resistance	Typ. 5 kΩ	
Switching threshold		
Low	<5 VDC	
High	>15 VDC	
Event counter		
Quantity	2	
Signal form	Square wave pulse	
Evaluation	Each falling edge, cyclic counter	
Input frequency	Max. 50 kHz	
Counter 1	Input 1	
Counter 2	Input 3	
Counter frequency	Max. 50 kHz	
Counter size	16-bit	
Gate measurement		
Quantity	1	
Signal form	Square wave pulse	
Evaluation	Rising edge - Falling edge	
Counter frequency		
Internal	48 MHz, 3 MHz, 187.5 kHz	
Counter size	16-bit	

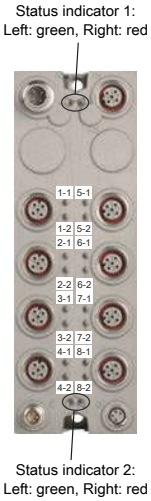
Table 2: X67DM1321.L12, X67DM1321.L12-1 - Technical data

Model number	X67DM1321.L12	X67DM1321.L12-1
Length of pause between pulses	≥100 µs	
Pulse length	≥20 µs	
Supported inputs	Input 2 or input 4	
Digital outputs		
Variant	FET positive switching	
Switching voltage	I/O power supply minus residual voltage	
Nominal output current	0.5 A	
Total nominal current	8 A	
Output circuit	Source	
Output protection	Thermal cutoff for overcurrent and short circuit, integrated protection for switching inductances, reverse polarity protection for output power supply	
Diagnostic status	Output monitoring with 10 ms delay	
Leakage current when switched off	5 µA	
Switching on after overload shutdown	Approx. 10 ms (depends on the module temperature)	
Residual voltage	<0.3 V at 0.5 A rated current	
Peak short-circuit current	<12 A	
Switching delay		
0 → 1	<400 µs	
1 → 0	<400 µs	
Switching frequency		
Resistive load	Max. 100 Hz	
Braking voltage when switching off inductive loads	50 VDC	
Electrical properties		
Electrical isolation	Channel isolated from bus Channel not isolated from channel	
Operating conditions		
Mounting orientation		
Any	Yes	
Installation elevation above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
Degree of protection per EN 60529	IP67	
Ambient conditions		
Temperature		
Operation	-25 to 60°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Mechanical properties		
Dimensions		
Width	53 mm	
Height	155 mm	
Depth	42 mm	
Weight	320 g	
Torque for connections		
M8	Max. 0.4 Nm	
M12	Max. 0.6 Nm	

Table 2: X67DM1321.L12, X67DM1321.L12-1 - Technical data

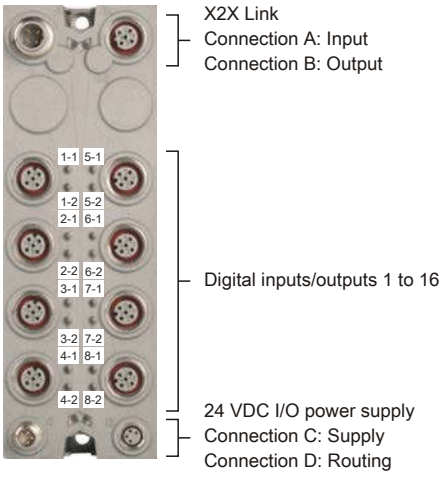
1) The power consumption of the sensors and actuators connected to the module is not permitted to exceed 12 W.

4 LED status indicators

Figure	LED	Color/Status		Description
	**Status indicator 1**: Status indicator for X2X Link			
	LED	**Green**	**Red**	**Description**
		Off	Off	No power supply via X2X Link
		On	Off	X2X Link supplied, communication OK
		Off	On	X2X Link supplied but X2X Link communication not functioning
		On	On	PREOPERATIONAL: X2X Link supplied, module not initialized
	I/O LEDs			
	LED	**Color**	**Status**	**Description**
	1/1 - 8/2	Orange	-	Output status of the corresponding digital input/output
	Status indicator 2: Status indicator for module function			
	LED	**Color**	**Status**	**Description**
	Left	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	Right	Red	Off	No power to module or everything OK
			On	Error or reset status
			Single flash	Warning/Error on an I/O channel. Level monitoring for digital outputs has been triggered.
			Double flash	Supply voltage not in the valid range

1) Depending on the configuration, a firmware update can take up to several minutes.

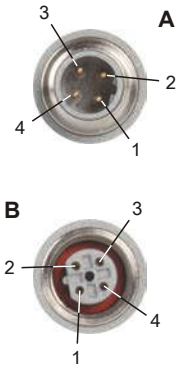
5 Connection elements



Left side / Channels 1 to 8 in the first byte		Right side / Channels 9 to 16 in the second byte	
Channel	**Connection**	**Connection**	**Channel**
1	1-1	5-1	9
2	1-2	5-2	10
...	...	...	...
7	4-1	8-1	15
8	4-2	8-2	16

6 X2X Link

This module is connected to X2X Link using pre-assembled cables. The connection is made using M12 circular connectors.

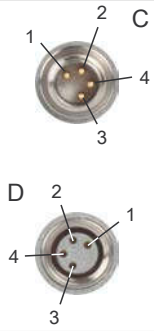
Connection	Pinout	
	**Pin**	**Description**
	1	X2X+
	2	X2X
	3	X2X⊥
	4	X2X\
	Shield connection made via threaded insert in the module. A → B-keyed (male), input B → B-keyed (female), output	

7 24 VDC I/O power supply

The I/O power supply is connected via M8 connectors C and D. The I/O power supply is connected via connector C (male). Connector D (female) is used to route the I/O power supply to other modules.

Information:

The maximum permissible current for the I/O power supply is 8 A (4 A per connection pin)!

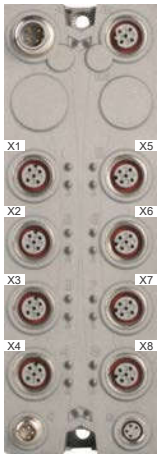
Connection	Pinout	
	**Pin**	**Name**
	1	24 VDC[1)]
	2	24 VDC[1)]
	3	GND
	4	GND
	C → Connector (male) in module, feed for I/O power supply D → Connector (female) in module, routing of I/O power supply	

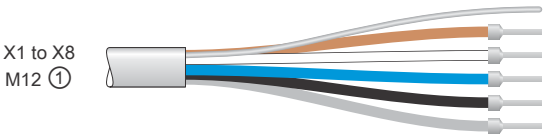
1) Both supply pins must be supplied. Cutting off the outputs is only ensured if **both** pins are disconnected from the power supply.

Information:

If the summation current of the outputs is >4 A, current must also be supplied via connector D, pin 2.

8 Pinout

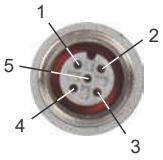




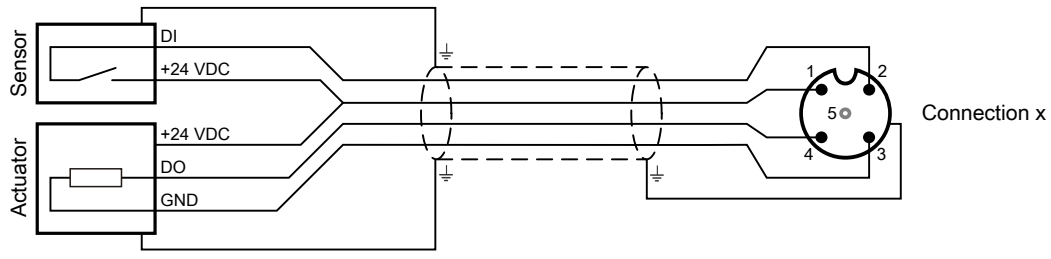
SHLD	
1	+24 VDC
2	DI/DO x-1
3	GND
4	DI/DO x-2
5	NC

① X67CA0A41.xxxx: M12 sensor cable, straight
X67CA0A51.xxxx: M12 sensor cable, angled

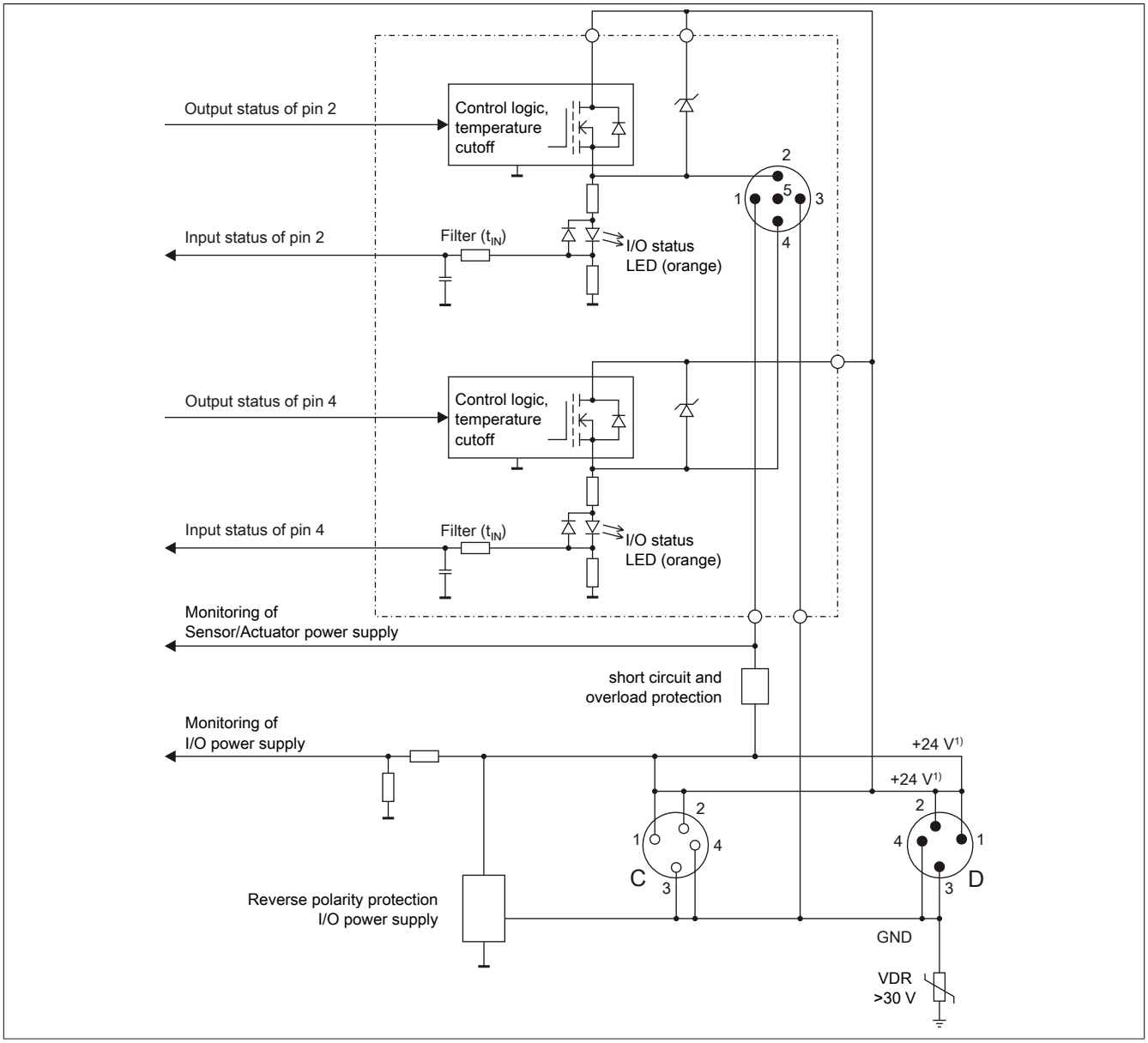
8.1 Connection X1 to X8

M12, 5-pin	Pinout		
Connection 1 to 4	Pin	Name	
		xxx.L12	xxx.L12-1
	1	24 VDC sensor/actuator power supply[1)]	
	2	Input/Output x-1	Input/Output x-2
	3	GND	
	4	Input/Output x-2	Input/Output x-1
	5	NC	
Connection 5 to 8	Shield connection made via threaded insert in the module. 1) Sensors/Actuators are not permitted to be supplied externally. X1 to X8 → A-keyed (female), input/output		

9 Connection example

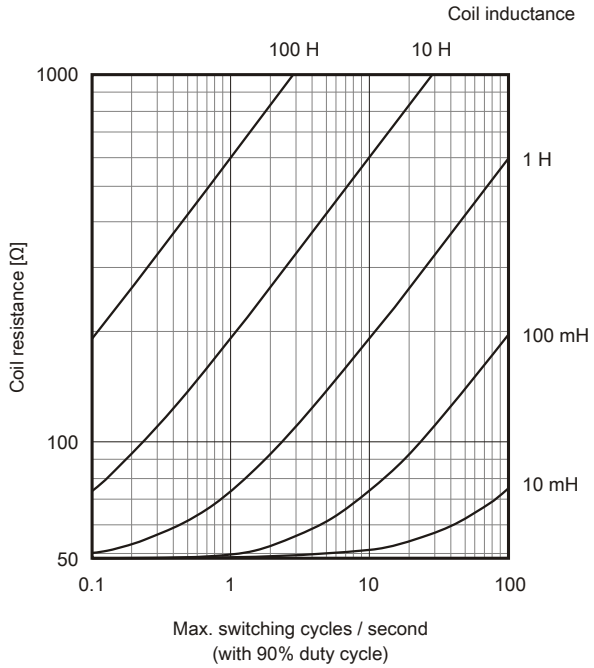


10 Input/Output circuit diagram



1) Cutting off the outputs is only ensured if **both** pins are disconnected from the power supply.

11 Switching inductive loads



12 Register description

12.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

These general data points are listed in section "Additional information - General data points" of the X67 system user's manual.

12.2 Function model 2 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
16	ConfigIOMask01	USINT				•
17	ConfigIOMask02	USINT				•
18	ConfigOutput03 (input filter)	USINT				•
Communication						
0	Input state of digital inputs 1 to 8	USINT	•			
	DigitalInput01	Bit 0				
	...	...				
	DigitalInput08	Bit 7				
1	Input state of digital inputs 9 to 16	USINT	•			
	DigitalInput09	Bit 0				
	...	...				
	DigitalInput16	Bit 7				
2	Switching state of digital outputs 1 to 8	USINT			•	
	DigitalOutput01	Bit 0				
	...	...				
	DigitalOutput08	Bit 7				
3	Switching state of digital outputs 9 to 16	USINT			•	
	DigitalOutput09	Bit 0				
	...	...				
	DigitalOutput16	Bit 7				
30	Status of digital outputs 1 to 8	USINT	•			
	StatusDigitalOutput01	Bit 0				
	...	...				
	StatusDigitalOutput08	Bit 7				
31	Status of digital outputs 9 to 16	USINT	•			
	StatusDigitalOutput09	Bit 0				
	...	...				
	StatusDigitalOutput16	Bit 7				
26	Input latch - Rising edges 1 to 8	USINT	•			
	InputLatch01	Bit 0				
	...	...				
	InputLatch08	Bit 7				
27	Input latch - Rising edges 9 to 16	USINT	•			
	InputLatch09	Bit 0				
	...	...				
	InputLatch16	Bit 7				
28	Acknowledgment - Input latch 1 to 8	USINT			•	
	QuitInputLatch01	Bit 0				
	...	...				
	QuitInputLatch08	Bit 7				
29	Acknowledgment - Input latch 9 to 16	USINT			•	
	QuitInputLatch09	Bit 0				
	...	...				
	QuitInputLatch16	Bit 7				
8192	asy_ModulID	UINT		•		
8196	asy_SupplyStatus	USINT		•		
8208	asy_SupplyInput	USINT		•		
8210	asy_SupplyOutput	USINT		•		

12.3 Function model 1 - Counter

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
16	ConfigIOMask01	USINT				•
17	ConfigIOMask02	USINT				•
20	ConfigOutput01 (counter channel 1)	USINT				•
22	ConfigOutput02 (counter channel 2)	USINT				•
18	ConfigOutput03 (input filter)	USINT				•
Communication						
0	Input state of digital inputs 1 to 8	USINT	•			
	DigitalInput01	Bit 0				
	...	...				
	DigitalInput08	Bit 7				
1	Input state of digital inputs 9 to 16	USINT	•			
	DigitalInput09	Bit 0				
	...	...				
	DigitalInput16	Bit 7				
2	Switching state of digital outputs 1 to 8	USINT			•	
	DigitalOutput01	Bit 0				
	...	..				
	DigitalOutput08	Bit 7				
3	Switching state of digital outputs 9 to 16	USINT			•	
	DigitalOutput09	Bit 0				
	...	..				
	DigitalOutput16	Bit 7				
30	Status of digital outputs 1 to 8	USINT	•			
	StatusDigitalOutput01	Bit 0				
	...	...				
	StatusDigitalOutput08	Bit 7				
31	Status of digital outputs 9 to 16	USINT	•			
	StatusDigitalOutput09	Bit 0				
	...	...				
	StatusDigitalOutput16	Bit 7				
26	Input latch - Rising edges 1 to 8	USINT	•			
	InputLatch01	Bit 0				
	...	...				
	InputLatch08	Bit 7				
27	Input latch - Rising edges 9 to 16	USINT	•			
	InputLatch09	Bit 0				
	...	...				
	InputLatch16	Bit 7				
28	Acknowledgment - Input latch 1 to 8	USINT			•	
	QuitInputLatch01	Bit 0				
	...	...				
	QuitInputLatch08	Bit 7				
29	Acknowledgment - Input latch 9 to 16	USINT			•	
	QuitInputLatch09	Bit 0				
	...	...				
	QuitInputLatch16	Bit 7				
4	Counter01	UINT	•			
6	Counter02	UINT	•			
20	Reset counter 1	USINT			•	
	ResetCounter01	Bit 5				
22	Reset counter 2	USINT			•	
	ResetCounter02	Bit 5				
8192	asy_ModulID	UINT		•		
8196	asy_SupplyStatus	USINT		•		
8208	asy_SupplyInput	USINT		•		
8210	asy_SupplyOutput	USINT		•		

12.4 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
16	-	ConfigIOMask01	USINT				•
17	-	ConfigIOMask02	USINT				•
20	-	ConfigOutput01 (counter channel 1)	USINT				•
22	-	ConfigOutput02 (counter channel 2)	USINT				•
18	-	ConfigOutput03 (input filter)	USINT				•
Communication							
0	0	Input state of digital inputs 1 to 16	UINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput16	Bit 15				
2	2	Switching state of digital outputs 1 to 16	UINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput16	Bit 15				
30	-	Status of digital outputs 1 to 16	UINT	•			
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput16	Bit 15				
26	-	Input latch - Rising edges 1 to 8	USINT	•			
		InputLatch01	Bit 0				
		...	...				
		InputLatch08	Bit 7				
27	-	Input latch - Rising edges 9 to 16	USINT	•			
		InputLatch09	Bit 0				
		...	...				
		InputLatch16	Bit 7				
28	-	Acknowledgment - Input latch 1 to 8	USINT			•	
		QuitInputLatch01	Bit 0				
		...	...				
		QuitInputLatch08	Bit 7				
29	-	Acknowledgment - Input latch 9 to 16	USINT			•	
		QuitInputLatch09	Bit 0				
		...	...				
		QuitInputLatch16	Bit 7				
4	-	Counter01	UINT		•		
6	-	Counter02	UINT		•		
20	-	Reset counter 1	USINT			•	
		ResetCounter01	Bit 5				
22	-	Reset counter 2	USINT			•	
		ResetCounter02	Bit 5				
8192	-	asy_ModulID	UINT		•		
8196	-	asy_SupplyStatus	USINT		•		
8208	-	asy_SupplyInput	USINT		•		
8210	-	asy_SupplyOutput	USINT		•		

1) The offset specifies the position of the register within the CAN object.

12.4.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use additional registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" of the X67 user's manual (version 3.30 or later).

12.4.2 CAN I/O bus controller

The module occupies 2 digital logical slots on CAN I/O.

12.5 Configuration

12.5.1 I/O mask 1 to 8

Name:
ConfigIOMask01

Channels are configured as inputs/outputs in this register. It also determines whether output monitoring or filtering is applied to the channels. Outputs are monitored but not filtered.

Information:

In counter operation, channels 1 to 4 can only be configured as inputs.

Data type	Values	Bus controller default setting
USINT	See bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	Channel 1 configured as input/output	0	Configured as input (bus controller default setting)
		1	Configured as output
...		...	
7	Channel 8 configured as input/output	0	Configured as input (bus controller default setting)
		1	Configured as output

12.5.2 I/O mask 9 to 16

Name:
ConfigIOMask02

Channels are configured as inputs/outputs in this register. It also determines whether output monitoring or filtering is applied to the channels. Outputs are monitored but not filtered.

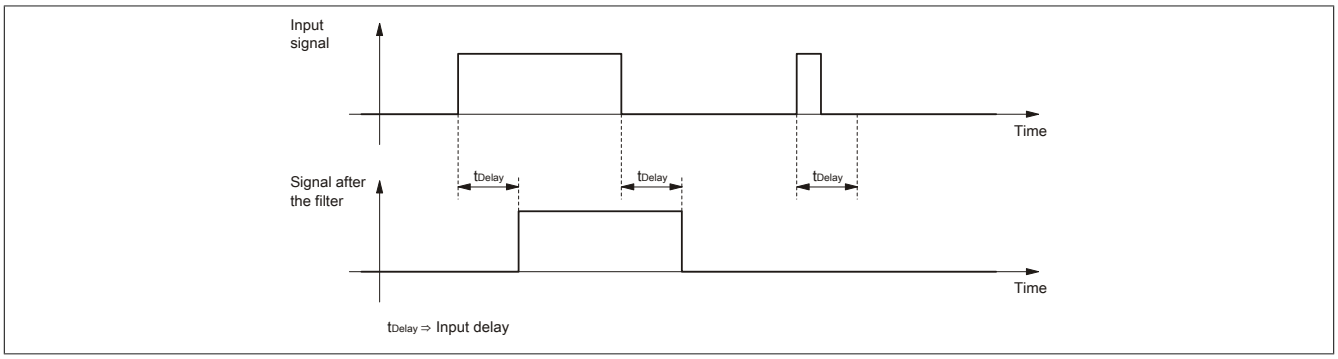
Data type	Values	Bus controller default setting
USINT	See bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	Channel 9 configured as input/output	0	Configured as input (bus controller default setting)
		1	Configured as output
...		...	
7	Channel 16 configured as input/output	0	Configured as input (bus controller default setting)
		1	Configured as output

12.5.3 Input filter

An input filter is available for each input. The input delay can be set using register "ConfigOutput03" on page 13. Disturbance pulses which are shorter than the input delay are suppressed by the input filter.



12.5.3.1 Digital input filter

Name:
ConfigOutput03

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs.

Data type	Value	Filter
USINT	0	No software filter (bus controller default setting)
	2	0.2 ms
	...	...
	250	25 ms - Higher values are limited to this value

12.5.4 Configuration of Counter Channels 1 and 2

Name:
ConfigOutput01 to ConfigOutput02
ResetCounter01 to ResetCounter02

Counter channels 1 and 2 are configured in this register.

Data type	Values	Bus controller default setting
USINT	See bit structure.	0

Bit structure:

Bit	Description	Value	Information
0 - 2	Configuration of the counter frequency (only with gate measurement)	000	Counter frequency = 48 MHz (bus controller default setting)
		001	Counter frequency = 3 MHz
		010	Counter frequency = 187.5 kHz
		011 to 111	Reserved
3 - 4	Reserved	0	
5	ResetCounter0x	0	No affect on counter (bus controller default setting)
		1	Delete counter
6 - 7	Configuration of the operating mode	0	Event counter operation (Bus controller default setting)
		1	Gate measurement

Event counter operation

The falling edges are registered on the counter input.

The counter status is collected with a fixed offset to the network cycle and transferred in the same cycle.

Gate measurement

> **Information:**
>
> **Only one of the counter channels at a time can be used for gate measurement.**

The time of rising to falling edges for the gate input is registered using an internal frequency. The result is checked for overflow (0xFFFF).

The recovery time between measurements must be >100 µs.

The measurement result is transferred with the falling edge to the result memory.

12.6 Communication

12.6.1 Digital inputs

Unfiltered

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

Filtered

The filtered status is collected with a fixed offset to the network cycle and transferred in the same cycle. Filtering takes place asynchronously to the network in multiples of 200 µs with a network-related jitter of up to 50 µs.

12.6.1.1 Input state of digital inputs 1 to 16

Name:
DigitalInput01 to DigitalInput16

This register indicates the input state of digital inputs 1 to 16.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input state - Digital input 1
...		...	
15	DigitalInput16	0 or 1	Input state - Digital input 16

12.6.1.2 Input state of digital inputs 1 to 8

Name:
DigitalInput01 to DigitalInput08

This register indicates the input state of digital inputs 1 to 8.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input state - Digital input 1
...		...	
7	DigitalInput08	0 or 1	Input state - Digital input 8

12.6.1.3 Input state of digital inputs 9 to 16

Name:
DigitalInput09 to DigitalInput16

This register indicates the input state of digital inputs 9 to 16.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalInput09	0 or 1	Input state - Digital input 9
...		...	
7	DigitalInput16	0 or 1	Input state - Digital input 16

12.6.2 Digital outputs

The output status is transferred to the output channels with a fixed offset in relation to the network cycle (SyncOut).

12.6.2.1 Switching state of digital outputs 1 to 16

Name:
DigitalOutput01 to DigitalOutput16

This register is used to store the switching state of digital outputs 1 to 16.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
15	DigitalOutput16	0	Digital output 16 reset
		1	Digital output 16 set

12.6.2.2 Switching state of digital outputs 1 to 8

Name:
DigitalOutput01 to DigitalOutput08

This register is used to store the switching state of digital outputs 1 to 8.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
7	DigitalOutput08	0	Digital output 08 reset
		1	Digital output 08 set

12.6.2.3 Switching state of digital outputs 9 to 16

Name:
DigitalOutput09 to DigitalOutput16

This register is used to store the switching state of digital outputs 9 to 16.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput09	0	Digital output 09 reset
		1	Digital output 09 set
...		...	
7	DigitalOutput16	0	Digital output 16 reset
		1	Digital output 16 set

12.6.3 Monitoring status of the digital outputs

On the module, the output states of the outputs are compared to the target states. The control of the output driver is used for the target state.

A change in the output state resets monitoring for that output. The status of each individual channel can be read. A change in the monitoring status generates an error message.

12.6.3.1 Status of digital outputs 1 to 16

Name:
StatusDigitalOutput01 to StatusDigitalOutput16

This register is used to indicate the status of digital outputs 1 to 16.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	StatusDigitalOutput01	0	Channel 01: No error
		1	Channel 01: Short circuit or overload
...		...	
15	StatusDigitalOutput16	0	Channel 16: No error
		1	Channel 16: Short circuit or overload

12.6.3.2 Status of digital outputs 1 to 8

Name:
StatusDigitalOutput01 to StatusDigitalOutput08

This register is used to indicate the status of digital outputs 1 to 8.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	StatusDigitalOutput01	0	Channel 01: No error
		1	Channel 01: Short circuit or overload
...		...	
7	StatusDigitalOutput08	0	Channel 08: No error
		1	Channel 08: Short circuit or overload

12.6.3.3 Status of digital outputs 9 to 16

Name:
StatusDigitalOutput09 to StatusDigitalOutput16

This register is used to indicate the status of digital outputs 9 to 16.

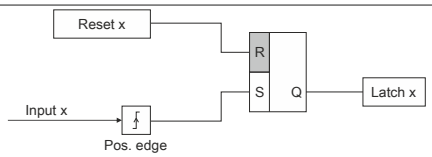
Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	StatusDigitalOutput09	0	Channel 09: No error
		1	Channel 09: Short circuit or overload
...		...	
7	StatusDigitalOutput16	0	Channel 16: No error
		1	Channel 16: Short circuit or overload

12.6.4 Input latch

It works in the same way as a dominant reset RS flip-flop.



R	S	Q	State
0	0	x	Do not change
0	1	1	Set
1	0	0	Reset
1	1	0	Reset

12.6.4.1 Input latch - Rising edges 1 to 8

Name:
InputLatch01 to InputLatch08

The rising edges of the input signal can be latched with a resolution of 200 µs in this register. The input latch is either reset or prevented from latching with register "QuitInputLatch0x" on page 17.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	InputLatch01	0	Do not latch input 1
		1	Latch input 1
...		...	
7	InputLatch08	0	Do not latch input 8
		1	Latch input 8

12.6.4.2 Input latch - Rising edges 9 to 16

Name:
InputLatch09 to InputLatch16

The rising edges of the input signal can be latched with a resolution of 200 µs in this register. The input latch is either reset or prevented from latching with register "QuitInputLatchxx" on page 18.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	InputLatch09	0	Do not latch input 9
		1	Latch input 9
...		...	
7	InputLatch16	0	Do not latch input 16
		1	Latch input 16

12.6.4.3 Acknowledgment - Input latch 1 to 8

Name:
QuitInputLatch01 to QuitInputLatch08

This register is used to reset the input latch by channel.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	QuitInputLatch01	0	Do not reset input 1
		1	Reset input 1
...		...	
7	QuitInputLatch08	0	Do not reset input 8
		1	Reset input 8

12.6.4.4 Acknowledgment - Input latch 9 to 16

Name:
QuitInputLatch09 to QuitInputLatch16

This register is used to reset the input latch by channel.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	QuitInputLatch09	0	Do not reset input 9
		1	Reset input 9
...		...	
7	QuitInputLatch16	0	Do not reset input 16
		1	Reset input 16

12.6.5 Event counter / Gate measurement

Name:
Counter01 and Counter02

Depending on the mode, this register contains the counter value or gate time of channel 1 and channel 2.

Data type	Values
UINT	0 to 65535

12.6.6 Reading the module ID

Name:
asy_ModulID

This register offers the possibility to read the module ID.

Data type	Values
UINT	Module ID

12.6.7 Operating limit status registers

Name:
asy_SupplyStatus

This register can be used to read the status of the operating limits.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Input supply within / outside of the warning limits	0	Within the warning limits (18 to 30 V)
		1	Outside of the warning limits (<18 V or >30 V)
1	Reserved	0	
2	Output supply within / outside of the warning limits	0	Within the warning limits (18 to 30 V)
		1	Outside of the warning limits (<18 V or >30 V)
3 - 7	Reserved	0	

12.6.8 I/O supply voltage

Name:
asy_SupplyInput

This register contains the I/O supply voltage measured by the module.

Data type	Values	Information
USINT	0 to 255	Resolution 1 V

12.6.9 Output supply voltage

Name:
asy_SupplyOutput

This register contains the output supply voltage measured by the module.

Data type	Values	Information
USINT	0 to 255	Resolution 1 V

12.7 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time	
Without filtering	150 µs
With filtering	200 µs
Counter operation	250 µs

12.8 Minimum cycle time

The minimum cycle time specifies the time up to which the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Without filtering	150 µs
With filtering	200 µs
Counter operation	250 µs