Silicon Power
INDUSTRIAL

Industrial

M.2 2242 NVMe Gen4x4 SSD

MEA3M0E Series

Datasheet



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Specifications Overview

- **Capacity**
  - 128GB, 256GB, 512GB, 1TB, 2TB
- **Form Factor**
  - M.2 2242
- **PCIe Interface**
  - PCIe Gen4x4
  - NVMe 1.4
- **Performance**
  - Sequential Read: up to 4730 MB/s
  - Sequential Write: up to 4410 MB/s
  - Random 4k Read: up to 858K IOPS
  - Random 4k Write: up to 632K IOPS
- **Temperature Range**
  - Operation temperature:
  - Normal Temperature: -20°C to +75°C
    Wide Temperature: -40°C to +85°C
  - Storage temperature: -40°C to +85°C
- **Power Consumption**
  - Supply Voltage: DC +3.3V ± 5%
  - Read (Max.): 1670 mA
  - Write (Max.): 1420 mA
  - Idle (Avg.): 220 mA
- **Reliability**
  - TBW:
    128GB: 321 TB
    256GB: 642 TB
    512GB: 1,284 TB
    1TB: 2,569 TB
    2TB: 5,137 TB
  - MTBF: > 3,000,000 hrs.
- **ECC Performance**
  - LDPC
- **Environment Specification**
  - Shock
  - Vibration
- **Compliant Specifications**
  - RoHS
- **Feature Support**
  - TCG Opal 2.0
  - AES-256
  - Write Protect
  - Quick Erase

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Revision History

Revision	Date	Major Changes
	2023/07/19	1. Preliminary release
1.0	2024/05/30	1. First release
1.1	2024/06/14	1. Update order information
1.2	2025/02/12	1. Update new FW BOM-code
1.3	2025/06/30	1. Update TBW

1. Product Description

1.1 Overview

Silicon Power Industrial's PCIe NVMe solid-state drive is a storage solution built on 3D NAND flash memory technology. The SSD employs an optimized wear-leveling algorithm to effectively extend its lifespan. Additionally, it ensures End-to-End Data Protection to safeguard data in transit, minimizing the risk of corruption, maintaining data integrity, and delivering reliable and secure storage solutions for users.

1.2 Features

- M.2 2242 form factor, M key
- PCI Express Base Specification Revision 4 standard with Gen4x4 8GB/s bandwidth
- NVME 2.0 command protocol
- Power shielding firmware architecture
- End-to-End data protection
- Global wear-leveling algorithm balances program/erase cycles
- Early weak block retirement
- Support SMART Toolbox for Windows and Linux
- Built-in dynamic temperature sensor with Thermal Throttling
- Dynamic SLC architecture
- Power shield firmware architecture
- Supports ASPM, L1.2
- AES 256 bit Hardware Self Encryption
- Trusted Computing Group (TCG) Opal protocol 2.0 (Optional)
- Supports in-field seamless FW update tool to keep the SSD’s original data (Optional)
- Conformal Coating - Standard IPC A-610E(Optional)

1.3 System Requirements

- Gen4x4 interface, in M.2 2242 standard form factor.
- Voltage: DC +3.3V ± 5%
- Operating System:
  -Windows
  -Linux

2. Specification

2.1 Physical Dimension

2.1.1 Dimension

The dimensions of M.2 2242 PCIe Gen4x4 SSD are illustrated in Figure 1 and described in Table 1.

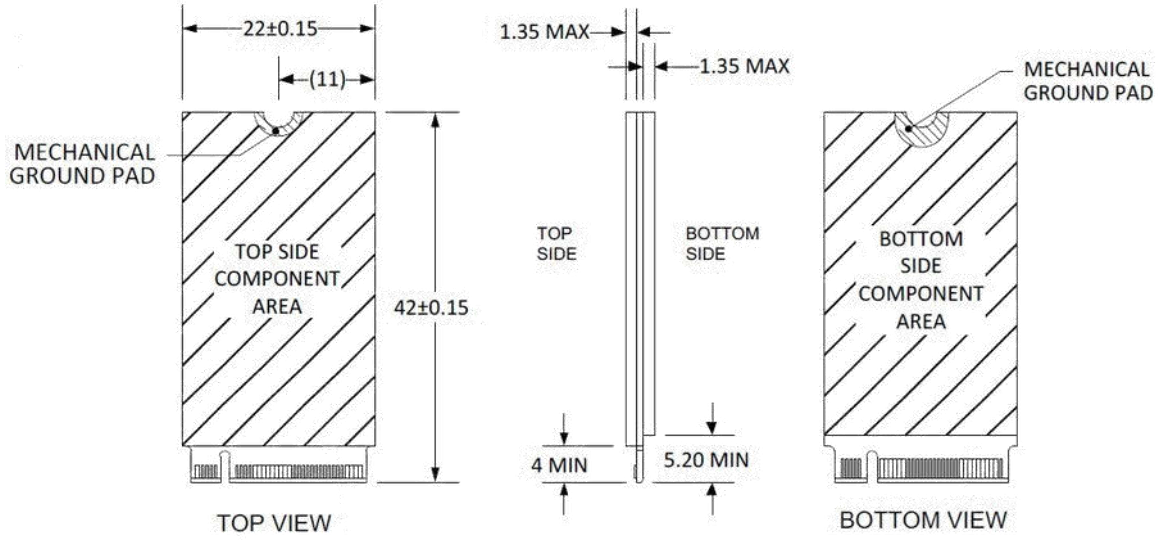

Figure 1 : M.2 2242 Gen4x4 SSD Dimensions

Table 1 : M.2 2242 Gen4x4 SSD Physical Dimension

Length	42±0.15mm
Width	22±0.15mm
Thickness(connector)	3.5mm

2.1.2 Weight

- 128GB: 2.5g±5%
- 256GB: 3.0g±5%
- 512GB: 3.5g±5%
- 1TB: 4.0g±5%
- 2TB: 4.0g±5%

2.2 Electrical Specifications

2.2.1 Operating Condition

- Supply Voltage: DC +3.3V ± 5%

Table 2 : Power Consumption

Mode		Power Consumption				Unit
	128GB	256GB	512GB	1TB	2TB	
Read (Max.)	550	1100	1300	1260	1670	mA
Write (Max.)	450	750	1050	1120	1420	mA
Idle (Avg.)	< 220	< 220	< 220	< 220	< 220	mA

Notice: The value is various bases on the capacity and the test platform.
Notice: Power consumption is measured during the sequential read and write operations performed by CrystalDiskMark5.5.0.
Notice: Power consumption of Idle is measured when the platform gets into a steady-state mode after IOMeter runs "Idle" script for 10mins.
※ Testing Platform: Mother-Board: MAG Z790, CPU: Intel(R) Core i5-14400 CPU 4GHz, Intel UHD Graphics 730, Main Memory: DDR5-4800 16GB X 1pcs, Operating System: Win 10, 64bit, Test Temperature: 25°C

2.3 Performance

2.3.1 Transfer Modes

- PCIe Gen4x4, backward compatible with PCIe Gen1 & PCIe Gen2 & PCIe Gen3.

2.3.2 TeraByte Write

Table 3 : TBW Data

Mode		TBW Data				Unit
	128GB	256GB	512GB	1TB	2TB	
Client	321	642	1,284	2,569	5,137	TB

Notice: TBW is estimated by formula **TBW = (Capacity x PE Cycles) x (1 + OP) x (WLE) / (WAF)**

- **OP = (Physical Capacity / Logical Capacity) - 1**
- **WLE =** It could be different depended on the workload or usage containing data size and access rate.
- **Client workload:** Sequential write workload.
- **Enterprise workload:** Follow JESD219A enterprise workload which is generated by VDBENCH script and tested by VDBENCH.

2.3.3 Wear-Leveling

- Enhanced endurance by global Wear-Leveling.

2.4 Environmental Conditions

Table 4 : Environmental Conditions

Feature	Operating	Non-Operating
Temperature (Normal Grade)	-20°C to +75°C	-55°C to +95°C
Temperature (Wide Grade)	-40°C to +85°C	-55°C to +95°C
Humidity	10% to 95% RH, non-condensing	
Vibration	20G (Peak-to-Peak), 80~2000 Hz	
Shock	1,500G, 0.5ms	

Notice:

- Vibration: Duration, 30 min x 3 axis.
- Shock: 1500G, 0.5msec, half-sine wave, 3 times in each direction, total = 18 times (6 directions).
- Temperature: The temperature reading is for the environment defined as Ta.

2.5 Reliability

Table 5 : Reliability

Feature	Specification
ECC Capability	Hardware LDPC ECC engine
MTBF	>3,000,000 hrs @25°C (MIL-HDBK-217F part count method Telcordia SR-332 Method)
Program / Erase Endurance	3,000 P/E cycles
Optimal sustained performance	Dynamic SLC Cache Architecture
Data Endurance & Data integrity	Early weak block retirement, Global Wear leveling
Data Retention	10% of program / Erase Endurance cycles: 10 Years
	100% of program / Erase Endurance cycles: 1 Years

Notice:

- Data retention: The value is based on normal program/erase endurance at room temperature. High environmental temperature may shorten the retention period.

2.6 Compliance Specifications

- RoHS
- Reach
- CE
- FCC

2.7 Technique

2.7.1 TCG Opal 2.0

The SLC cache technology divides a cache space in the TLC device to be simulated as an SLC, and the speed in TCG/Opal stands for Trusted Computing Group Opal. The Trusted Computing Group is an organization that develops open standards for trusted computing platforms. The latest Opal Storage Specification is currently available in version 2.0, featuring a demand encryption function for the stored data so that an unauthorized person will not be able to see or access the data, even if possession of a drive was gained.

2.7.2 Thermal Throttling

SP Industrial SSD started implementing a new generation control mechanism of thermal throttling with multiple levels of temperature control. The major benefit of new generation control mechanisms avoids sudden change of SSD performance to get the better balance between performance and thermal management.

2.7.3 Wide Temperature

Products for industrial applications often have to withstand extreme temperature conditions. SP Industrial offers solutions that are able to operate in all systems and environments, including harsh operating environments and industries such as defense and telecommunications. Select SSD controllers from SP Industrial are equipped with wide temperature technology to operate reliably from a wide temperature range of -40°C to +85°C.

2.7.4 Write Protect

The Industrial M.2 NVMe SSD contains a feature connector for Write Protect mode. Write Protect mode is enabled when the Write Protect feature connector is placed at 1.27mm pitch Pin Header after power up or any time. During Write Protect mode, the SSD is read-only and data can’t be written to it. If no feature connector is placed, data can be written as usual.

2.7.5 Quick Erase

Reliably erasing data from storage media is a critical component of secure data management. Flash-based solid-state drives (SSDs) differ from hard drives in both the technology they use to store data (flash chips vs. magnetic disks) and the algorithms they use to manage and access that data. SSDs maintain a layer of indirection between the logical block addresses that computer systems use to access data and the raw flash addresses that identify physical storage. The layer of indirection enhances SSD performance and reliability by hiding the flash memory’s idiosyncratic interface and managing its limited lifetime. However, it can also produce copies of the data that are invisible to the user but recoverable by a sophisticated attacker. For this reason, it is so important to sanitize the media completely.

2.7.6 Power Shield

The principle of SSD is Power Shield (PS) activates when the external voltage drops to a specific low level, such as from 3.3V to 2.7V. The voltage detection circuit (Voltage Detector) inside the controller will initiate the power supply protection function. When the SSD is operating and the DRAM is powered by an external power

supply, the data will be temporarily stored in the DRAM. During the power-off process, the command is sent from the host to the SSD controller to signal that the power is about to be interrupted, and the SSD controller will send confirmation messages to the host, and then transfer the data temporarily stored in the DRAM cache to the Flash Memory. This safeguards the internal firmware and data of the Flash memory from being damaged.

2.7.7 pSLC

To fill the gap between SLC and MLC/3D TLC solutions, SP Industrial offers pseudo-SLC (pSLC) Flash. It is an advanced variant of MLC/3D TLC that outperforms the latter in speed, program erase cycles, and overall reliability. Pseudo-SLC operates similar to SLC, but with fewer program erase cycles, which makes it a cost-effective alternative to SLC SP Industrial's latest Industrial SSD with pSLC solution.

2.7.8 SLC Cache

The SLC cache technology divides a cache space in the TLC device to be simulated as an SLC, and the speed in the SLC cache can be improved. But when the cache space is run out, the speed will return to the original TLC speed.

2.7.9 Bad Block Management

Bad Block Management is a mechanism for bad blocks implemented by the controller to detect and mark the bad blocks in the flash memory, and it uses reserved spare blocks to replace the bad blocks to prevent the data from being written into the bad block again. Bad Block Management improves the reliability and endurance of data access.

2.7.10 Garbage Collection

SSD uses the storage technology of flash memory (NAND flash). The principle of SSD is that the controller stores the data to be written in the Flash memory. When writing data, the SSD must first erase the data in the old block before writing new data. That is, the new data cannot directly cover the old invalid data. For SSD, Garbage Collection refers to the process of re-transferring existing data to other NAND flash locations and erasing useless data.

2.7.11 Over Provisioning

OP is a firmware technology, mainly reserved by a part of the hard disk storage capacity in the physical partition of the SSD for the controller to use as cache. Over-provisioning improves performance and increases the endurance of an SSD, helping to extend the life of a hard drive.

2.7.12 Wear Leveling

For today's NAND flash devices, the main limitation is Program/Erase lifespan (number of P/E cycles). The key solution for this constraint is to manage the attrition rate in the entire NAND flash device so that each block will be evenly distributed. Therefore, efficient management of wear in whole blocks is required in order to maximize the lifespan of a NAND flash device. To accomplish this, one method is to manage the P/E cycle of each block individually, which will help to regularly distribute them and avoid overlaying on some blocks. This method is called wear leveling.

3. Functional Description

3.1 Architecture

SILICON POWER'S M.2 2242 PCIe Gen4x4 MEA3M0E series is designed to operate and work as data or code storage device by NAND Flash memory and its controller through Standard Gen4x4 8GB/s interface to host systems.

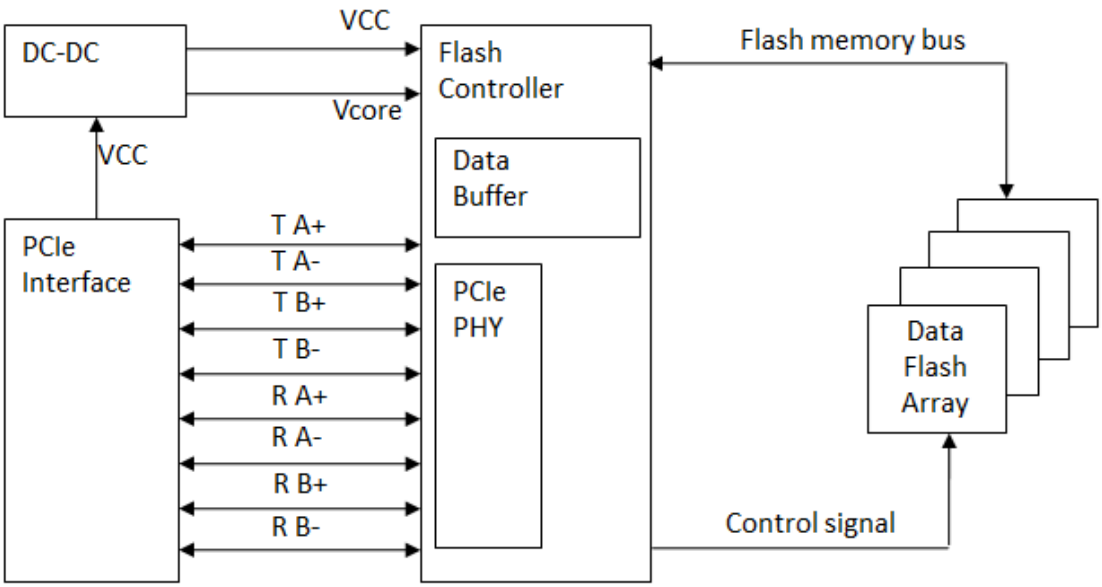

Figure 2 : M.2 2242 PCIe Gen4x4 MEA5M0E Series Block Diagram

3.2 Signal Assignment

The signals assigned for M.2 2242 PCIe applications are described in the following Table and Figure.

	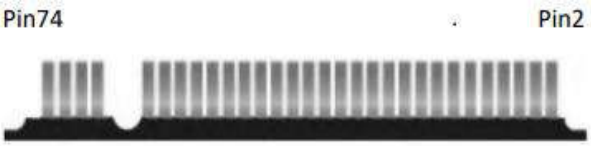
Front	**Rear**

Figure 3 : M.2 2242 PCIe Signal Connector

Table 6 : M.2 2242 PCIe Connector Pin Definitions

Name	Pin	Pin	Name
GND	01	02	+3.3V
GND	03	04	+3.3V
PETn3	05	06	NC
PETp3	07	08	NC
GND	09	10	LED1#
PERn3	11	12	+3.3V
PERp3	13	14	+3.3V
GND	15	16	+3.3V
PETn2	17	18	+3.3V
PETp2	19	20	NC
GND	21	22	NC
PERn2	23	24	NC
PERp2	25	26	NC
GND	27	28	NC
PETn1	29	30	NC
PETp1	31	32	NC
GND	33	34	NC
PERn1	35	36	NC
PERp1	37	38	NC
GND	39	40	NC
PETn0	41	42	NC
PETp0	43	44	NC
GND	45	46	NC
PERn0	47	48	NC
PERp0	49	50	PERST#
GND	51	52	CLKREQ#
REFCLKn	53	54	PEWAKE
REFCLKp	55	56	Reserved
GND	57	58	Reserved
Module Key	59	60	Module Key
Module Key	61	62	Module Key
Module Key	63	64	Module Key
Module Key	65	66	Module Key
NC	67	68	NC

PEDET	69	70	+3.3V
GND	71	72	+3.3V
GND	73	74	+3.3V
GND	75	N/A	N/A

3.3 NVMe Command List

Table 7 : Admin Commands

Command Name	O/M	Code
Delete I/O Submission Quene	M	00h
Create I/O Submission Quene	M	01h
Get Log Page	M	02h
Delete I/O Completion Quene	M	04h
Create I/O Completion Quene	M	05h
Identify	M	06h
Abort	M	08h
Set Features	M	09h
Get Features	M	0Ah
Asynchronous Event Request	M	0Ch
Firmware Commit	O	10h
Firmware Image Download	O	11h
Device Self-test	O	14h
Format NVMe	O	80h
Security Send	O	81h
Security Receive	O	82h
Sanitize	O	84h

Notice:

- M: Must
- O: Option

Table 8 : NVM Commands

Command Name	Code
Flush	00h
Write	01h
Read	02h
Write Uncorrectable	04h
Write Zeroes	08h
Dataset Management	09h
Verify	0Ch

Table 9 : Set Feature Commands

Command Name	O/M	Code
Reserved	-	00h
Arbitration	M	01h
Power Management	M	02h
LBA Range Type	O	03h
Temperature Threshold	M	04h
Error Recovery	M	05h
Volatile Write Cache	O	06h
Number of Queues	M	07h
Interrupt Coalescing	M	08h
Interrupt Vector Configuration	M	09h
Write Atomicity Normal	M	0Ah
Asynchronous Event Configuration	M	0Bh
Autonomous Power State Transition	O	0Ch
Host Memory Buffer	O	ODh
Timestamp	O	0Eh
Host Controlled Thermal Management	O	10h
Non-Operational Power State Configuration	O	11h
Software Progress Marker	O	80h

Table 10 : Get Log Page Commands

Command Name	O/M	Code
Reserved	-	00h
Error Information	M	01h
SMART/Health Information	M	02h
Firmware Slot Information	M	03h
Changed Namespace List	O	04h
Device Self-test	O	06h
Reserved	-	09h - 7Fh
Sanitize Status	O	81h
Reserved	-	82h - FFh

Table 11 : NVMe Commands

Command Name	Code
Flush	00h
Write	01h
Read	02h
Write Uncorrectable	04h
Compare	05h
Write Zeroes	08h
Dataset Management	09h

3.4 Device Identification

The following is the device identify table.

Table 12 : Identify Device Information

Bytes	O/M	Default Value	Description
01:00	M	0x1987	PCI Vendor ID (VID)
03:02	M	0x1987	PCI Subsystem Vendor ID (SSVID)
23:04	M	SN	Serial Number (SN)
63:24	M	Model Number	Model Number (MN)
71:64	M	FW Name	Firmware Revision (FR)
72	M	0x01	Recommended Arbitration Burst (RAB)
75:73	M	0	IEEE OUI Identifier (IEEE)
76	O	0x00	Controller Multi-Path I/O and Namespace Sharing Capabilities (CMIC)
77	M	0x09	Maximum Data Transfer size (MDTS)
79:78	M	0x0000	Controller ID (CNTLID)
83:80	M	0x00010200	Version (VER)
87:84	M	0x00124F80	RTD3 Resume Latency (RTD3R)
91:88	M	0x0016E360	RTD3 Entry Latency (RTD3E)
95:92	M	0	Optional Asynchronous Events Supported (OAES)
239:96	-	0	Reserved
255:240	-	0	Refer to the NVMe Management Interface Specification for definition
257:256	M	0x0007	Optional Admin Command Support (OACS)
258	M	0x03	Abort Command Limit (ACL)
259	M	0x03	Asynchronous Event Request Limit (AERL)
260	M	0x02	Firmware Updates (FRMW)
261	M	0x03	Log Page Attributes (LPA)
262	M	0x3F	Error Log Page Entires (ELPE)
263	M	0x04	Number of Power States Support (NPSS)
264	M	0x01	Admin Vendor Specific Command Configuration (AVSCC)
265	O	0x01	Autonomous Power State Transition Attribute (APSTA)
267:266	M	0x0157	Warning Composite Temperature Threshold (WCTEMP)
269:268	M	0x0193	Critical Composite Temperature Threshold (CCTEMP)
271:270	O	0x0000	Maximum Time for Firmware Activation (MTFA)
257:272	O	0	Host Memory Buffer Preferred Size (HMPRE)
279:276	O	0	Host Memory Buffer Minimum Size (HMMIN)
295:280	O	0	Total NVM Capacity (TNVMCAP)
311:296	O	0	Unallocated NVM Capacity (UNVMCAP)

315:312	O	0	Reply Protected Memory Block Support (RPMBS)
NVM Command Set Attributes			
511:316	-	0	Reserved
512	M	0x66	Submission Quene Entry Size (SQES)
513	M	0x44	Completion Quene Entry Size (CQES)
515:514	-	0	Reserved
519:516	M	0x01	Number of Namespaces (NN)
521:520	M	0x001E	Optional NVM Command Support (ONCS)
523:522	M	0	Fused Operation Support (FUSES)
524	M	0	Format NVM Attributes (FNA)
525	M	0x01	Volatile Write Cache (VWC)
527:526	M	0x00FF	Atomic Write Unit Normal (AWUN)
529:528	M	0x00	Atomic Write Unit Power Fail (AWUPF)
530	M	0x01	NVM Vendor Specific Command Configuration (NVSCC)
531	M	0	Reserved
533:532	O	0x00	Atomic Compare & Write Unit (ACWU)
535:534	M	0	Reserved
539:536	O	0x00	SGL Support (SGLS)
703:540	M	0	Reserved
IO Command Set Attributes			
2047:704	M	0	Reserved
2048:2079	M	PSD0	Power State 0 Descriptor
2111:2080	O	PSD1	Power State 1 Descriptor
2143:2112	O	PSD2	Power State 2 Descriptor
2175:2144	O	PSD3	Power State 3 Descriptor
2207:2176	O	PSD4	Power State 4 Descriptor
…	-	0000h	(N/A)
3071:3040	O	PSD31	Power State 31 Descriptor
Vendor Specific (VS)			
4095:3072	O	Reserved	Vendor Specific (VS)

3.5 SMART Attribute

The following table lists the SMART attributes supported by SP Industrial PCIe NVMe SSD.

Table 13 : SMART Attributes

# of Bytes	Byte Index	Attributes	Description
1	0	**Critical Warning:**. **Bit Definition** 00: If set to '1', then the available spare space has fallen below the threshold. 01: If set to '1', then a temperature is above an over temperature threshold or below an under temperature threshold. 02: If set to '1', then the NVM subsystem reliability has been degraded due to significant media related errors or any internal error that degrades NVM subsystem reliability. 03: If set to '1', then the media has been placed in read only mode. 04: If set to '1', then the volatile memory backup device has failed. This field is only valid if the controller has a volatile memory backup solution. 07:05: Reserved	This field indicates critical warnings for the state of the controller. Each bit corresponds to a critical warning type; multiple bits may be set. If a bit is cleared to '0', then that critical warning does not apply. Critical warnings may result in an asynchronous event notification to the host. Bits in this field represent the current associated state and are not persistent
2	2:1	**Composite Temperature:**	Contains a value corresponding to a temperature in degrees Kelvin that represents the current composite temperature of the controller and namespace(s) associated with that controller. The manner in which this value is computed is implementation specific and may not represent the actual temperature of any physical point in the NVM subsystem. The value of this field may be used to trigger an asynchronous event. Warning and critical overheating composite temperature threshold values are reported by the WCTEMP and CCTEMP fields in the Identify Controller data structure.
1	3	**Available Spare:**.	Contains a normalized percentage (0 to 100%) of the remaining spare capacity available
1	4	**Available Spare Threshold:**	When the Available Spare falls below the threshold indicated in this field, an asynchronous event completion may occur. The value is indicated as a normalized percentage (0 to 100%).
1	5	**Percentage Used:** .	Contains a vendor specific estimate of the percentage of NVM subsystem life used based on the actual usage and the manufacturer's prediction of NVM life. A value of 100 indicates that the estimated endurance of the NVM in the NVM subsystem has been consumed, but may not indicate an NVM subsystem failure. The value is allowed to exceed 100. Percentages greater than 254 shall be represented as 255. This value shall be updated once per power-on hour (when the controller is not in a sleep state). Refer to the JEDEC JESD218A standard for SSD device life and endurance measurement techniques
	31:6	Reserved	

16	47:32	**Data Units Read:**	Contains the number of 512 byte data units the host has read from the controller; this value does not include metadata. This value is reported in thousands (i.e., a value of 1 corresponds to 1000 units of 512 bytes read) and is rounded up. When the LBA size is a value other than 512 bytes, the controller shall convert the amount of data read to 512 byte units. For the NVM command set, logical blocks read as part of Compare and Read operations shall be included in this value.
16	63:48	**Data Units Written:**	Contains the number of 512 byte data units the host has written to the controller; this value does not include metadata. This value is reported in thousands (i.e., a value of 1 corresponds to 1000 units of 512 bytes written) and is rounded up. When the LBA size is a value other than 512 bytes, the controller shall convert the amount of data written to 512 byte units. For the NVM command set, logical blocks written as part of Write operations shall be included in this value. Write Uncorrectable commands shall not impact this value.
16	79:64	**Host Read Commands:**	Contains the number of read commands completed by the controller. For the NVM command set, this is the number of Compare and Read commands.
16	95:80	**Host Write Commands:**	Contains the number of write commands completed by the controller. **For the NVM command set, this is the number of Write commands.**
16	111:96	**Controller Busy Time:**	Contains the amount of time the controller is busy with I/O commands. The controller is busy when there is a command outstanding to an I/O Queue (specifically, a command was issued via an I/O Submission Queue Tail doorbell write and the corresponding completion queue entry has not been posted yet to the associated I/O Completion Queue). This value is reported in minutes.
16	127:112	**Power Cycles: Contains the number of power cycles.**	
16	143:128	**Power On Hours:**	Contains the number of power-on hours. Power on hours is always logging, even when in low power mode.
16	159:144	**Unsafe Shutdowns:**	Contains the number of unsafe shutdowns. This count is incremented when a shutdown notification (CC.SHN) is not received prior to loss of power.
16	175:160	**Media and Data Integrity Errors:**	Contains the number of occurrences where the controller detected an unrecovered data integrity error. Errors such as uncorrectable ECC, CRC checksum failure, or LBA tag mismatch are included in this field.
16	191:176	**Number of Error Information Log Entries:**	Contains the number of Error Information log entries over the life of the controller.
4	195:192	**Warning Composite Temperature Time:**	Contains the amount of time in minutes that the controller is operational and the Composite Temperature is greater than or equal to the Warning Composite Temperature Threshold (WCTEMP) field and less than the Critical Composite Temperature Threshold (CCTEMP) field in the Identify Controller data structure. If the value of the WCTEMP or CCTEMP field is 0h, then this field is always cleared to 0h regardless of the Composite Temperature value.

4	199:196	**Critical Composite Temperature Time:**	Contains the amount of time in minutes that the controller is operational and the Composite Temperature is greater the Critical Composite Temperature Threshold (CCTEMP) field in the Identify Controller data structure. If the value of the CCTEMP field is 0h, then this field is always cleared to 0h regardless of the Composite Temperature value.
16	215:200	**Temperature Sensor1-8**	Not support
4	219:216	**Thermal Management Temperature 1 Transition Count**	The number of times the controller manufacturer has entered the first stage
4	223:220	**Thermal Management Temperature 2 Transition Count**	Customized by the controller manufacturer, the number of times to enter the second stage
4	227:224	**Total Time For Thermal Management Temperature 1**	Customized by the controller manufacturer, the time to enter the first stage, unit is second
4	231:228	**Total Time For Thermal Management Temperature 2**	Customized by the controller manufacturer, the time to enter the second stage, unit is second
280	511:232	**Reserved**	

4. Ordering Information

4.1 Part Number Definition

Table 14 : Part Number Definition

Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	S	P	0	2	0	T	I	M	E	A	3	M	5	E	W	0

Code 1-2: Brand	SP: Silicon Power
Code 3-6: Capacity	128G: 128GB; 256G: 256GB; 512G: 512GB; 010T: 1TB; 020T: 2TB
Code 7: Product	I: Industrial Grade Product
Code 8-10: Type & Form Factor	MEA: PCIe 2242
Code 11-13: Model Series	3M5 Series: WD (3D TLC)
Code 14: SSD Series	E: DRAM-Less
Code 15: Operation Temperature	V: Normal Temperature W: Wide Temperature
Code 16: Reserved	0: Standard

4.2 Standard M.2 2242 NVMe Gen4x4 SSD MEA3M0E Series Information

Table 15 : Ordering information

Capacity	Part Number	BOM Code	Description	R/W Performance	
				Maximum (MB/s)	IOPS
Normal Temperature (-20°C ~75°C)					
128GB	SP128GIMEA3M5EV0	128GIMEA3M5EV0-010	BiCS5 1Tb*1	1450 / 850	831K / 166K
	SP128GIMEA3M5EV0	128GIMEA3M5EV0-020	BiCS5 1Tb*1	1480 / 860	832K / 180K
256GB	SP256GIMEA3M5EV0	256GIMEA3M5EV0-010	BiCS5 1Tb*2	3150 / 1600	843K / 324K
	SP256GIMEA3M5EV0	256GIMEA3M5EV0-020	BiCS5 1Tb*2	3135 / 1645	838K / 328K
512GB	SP512GIMEA3M5EV0	512GIMEA3M5EV0-010	BiCS5 2Tb*2	4250 / 3200	858K / 609K
	SP512GIMEA3M5EV0	512GIMEA3M5EV0-020	BiCS5 2Tb*2	4260 / 3275	828K / 644K
1TB	SP010TIMEA3M5EV0	010TIMEA3M5EV0-010	BiCS5 4Tb*2	4520 /3280	835K / 632K
2TB	SP020TIMEA3M5EV0	020TIMEA3M5EV0-010	BiCS5 8Tb*2	4730 /4410	830K /622K
Wide Temperature (-40°C ~85°C)					
128GB	SP128GIMEA3M5EW0	128GIMEA3M5EW0-010	BiCS5 1Tb*1	1480 / 860	832K / 180K

256GB	SP256GIMEA3M5EW0	256GIMEA3M5EW0-010	BiCS5 1Tb*2	3150 / 1600	843K / 324K
512GB	SP512GIMEA3M5EW0	512GIMEA3M5EW0-010	BiCS5 2Tb*2	4250 / 3200	858K / 609K
1TB	SP010TIMEA3M5EW0	010TIMEA3M5EW0-010	BiCS5 4Tb*2	4520 /3280	835K / 632K
2TB	SP020TIMEA3M5EW0	020TIMEA3M5EW0-010	BiCS5 8Tb*2	4730 /4410	830K /622K

4.3 Appendix

Table 16 : Abbreviation

Item	Abbreviation	Description
1	PCIe	Peripheral Component Interconnect Express
2	NVMe	Non-Volatile Memory Express
3	Gen	Generation
4	TBW	Tera Byte Write
5	MTBF	Mean Time Between Failures
6	LDPC	Low Density Parity Check
7	RAID	Redundant Array of Independent Drives
8	ECC	Error Correction Code
9	TCG	Trusted Computing Group
10	SMART	Self-Monitoring Analysis and Reporting Technology
11	FDE	Full Disk Encryption
12	AES	Advanced Encryption Standard
13	SLC	Single-Level Cell
14	SSD	Solid State Disk
15	OP	Over Provisioning
16	PS	Power Shield
17	DC	Direct Current
18	LED	Light Emitting Diode
19	DRAM	Dynamic Random Access Memory
20	PE	Program/Erase
21	WAF	Write Amplification Factor
22	WLE	Wear Leveling Efficiency
23	Ta	Ambient Temperature
24	LBA	Logical Block Address

Contact Information

Silicon Power Computer & Communications Incorporation, a solid state memory or storage business company, provides total solutions in the design and marketing of SSD, Flash Module, and Industry Card products. For further supporting or detail information related to the products, please inform us through the following contact email address: isupport@silicon-power.com. We will response the requests soon.