Approval Sheet

Customer	
Product Number	**M2SK-1GMF5C06-M**
Module speed	**PC2-6400**
Pin	**200 Pin**
CL-tRCD-tRP	**6-6-6**
Operating Temp	**0**°C ~ **85**°C
Date	**26th September 2018**

Rev 1.2

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The Total Solution For Industrial Flash Storage

1. Features

Key Parameter

Industry Nomenclature	Data Rate MT/s			tRCD (ns)	tRP (ns)	tRC (ns)
	CL=4	CL=5	CL=6			
PC2-6400	533	667	800	15	15	60

- JEDEC Standard 200-pin Small Outline Dual In-Line Memory Module
- Intend for 400MHz applications
- Inputs and Outputs are SSTL-18 compatible
- VDD=VDDQ= 1.8 Volt ± 0.1
- Differential clock input
- All inputs are sampled at the positive going edge of the system clock
- Bi-Directional data strobe with one clock cycle preamble and one-half clock post-amble
- Address and control signals are fully synchronous to positive clock edge.
- Auto Refresh and Self Refresh Modes support.
- Serial Presence Detect with EEPROM
- Automatic and controlled precharge commands.
- 14/10/1 Addressing (row/column/rank)-1GB
- Auto & self refresh 7.8μs (Tc ≤ +85°C)
- Golden Contactor
- SDRAM Operation Temperature
  - 0°C ≤ Tc ≤ +85°C
- Programmable Device Operation:
  - Burst Type: Sequential or Interleave
  - Operation: Burst Read and Write
  - Device CAS# Latency: 4,5,6
  - Burst Length: 4, 8
- RoHS Compliant *(Section 14)*

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2. Environmental Requirements

DDR2 SODIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
TOPR	Operating Temperature (ambient)	0 to +65	°C	1
TSTG	Storage Temperature	-50 to +100	°C	1
HOPR	Operating Humidity (relative)	10 to 90	%	
HSTG	Storage Humidity (without condensation)	5 to 95	%	1
PBAR	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1,2

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.
3. The component maximum case temperature (Tcase) shall not exceed the value specified in the DDR2 DRAM component specification.
Following JEDEC specifications.

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3. Ordering Information

DDR2 SODIMM						
Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank	ECC
M2SK-1GMF5C06-M	1GB	PC2-6400	128M x64	8	1	N/A

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4. Pin Configurations (Front side/Back side)

–x64 SODIMM

Front								Back							
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREF	51	DQS2	101	A1	151	DQ42	2	VSS	52	DM2	102	A0	152	DQ46
3	VSS	53	VSS	103	VDD	153	DQ43	4	DQ4	54	VSS	104	VDD	154	DQ47
5	DQ0	55	DQ18	105	A10/AP	155	VSS	6	DQ5	56	DQ22	106	BA1	156	VSS
7	DQ1	57	DQ19	107	BA0	157	DQ48	8	VSS	58	DQ23	108	/RAS	158	DQ52
9	VSS	59	VSS	109	/WE	159	DQ49	10	DM0	60	VSS	110	/S0	160	DQ53
11	/DQS0	61	DQ24	111	VDD	161	VSS	12	VSS	62	DQ28	112	VDD	162	VSS
13	DQS0	63	DQ25	113	/CAS	163	NC	14	DQ6	64	DQ29	114	ODT0	164	CK1
15	VSS	65	VSS	115	NC, /S1	165	VSS	16	DQ7	66	VSS	116	A13, NC	166	/CK1
17	DQ2	67	DM3	117	VDD	167	/DQS6	18	VSS	68	/DQS3	118	VDD	168	VSS
19	DQ3	69	NC	119	NC, ODT1	169	DQS6	20	DQ12	70	DQS3	120	NC	170	DM6
21	VSS	71	VSS	121	VSS	171	VSS	22	DQ13	72	VSS	122	VSS	172	VSS
23	DQ8	73	DQ26	123	DQ32	173	DQ50	24	VSS	74	DQ30	124	DQ36	174	DQ54
25	DQ9	75	DQ27	125	DQ33	175	DQ51	26	DM1	76	DQ31	126	DQ37	176	DQ55
27	VSS	77	VSS	127	VSS	177	VSS	28	VSS	78	VSS	128	VSS	178	VSS
29	/DQS1	79	CKE0	129	/DQS4	179	DQ56	30	CK0	80	CKE1	130	DM4	180	DQ60
31	DQS1	81	VDD	131	DQS4	181	DQ57	32	/CK0	82	VDD	132	VSS	182	DQ61
33	VSS	83	NC	133	VSS	183	VSS	34	VSS	84	NC	134	DQ38	184	VSS
35	DQ10	85	NC/BA2	135	DQ34	185	DM7	36	DQ14	86	NC/A14	136	DQ39	186	/DQS7
37	DQ11	87	VDD	137	DQ35	187	VSS	38	DQ15	88	VDD	138	VSS	188	DQS7
39	VSS	89	A12	139	VSS	189	DQ58	40	VSS	90	A11	140	DQ44	190	VSS
41	VSS	91	A9	141	DQ40	191	DQ59	42	VSS	92	A7	142	DQ45	192	DQ62
43	DQ16	93	A8	143	DQ41	193	VSS	44	DQ20	94	A6	144	VSS	194	DQ63
45	DQ17	95	VDD	145	VSS	195	SDA	46	DQ21	96	VDD	146	/DQS5	196	VSS
47	VSS	97	A5	147	DM5	197	SCL	48	VSS	98	A4	148	DQS5	198	SA0
49	/DQS2	99	A3	149	VSS	199	VDDSPD	50	NC	100	A2	150	VSS	200	SA1

Notes:

1. Pin 85 is NC for 1GB and BA2 for 2GB, 4GB.
2. Pin 86 is NC for 1GB, 2GB and A14 for 4GB.
3. Pin 115&119 NC for 1 rank and /S1, ODT1 for 2 rank.

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5. Architecture

Pin Definition

Pin Name	Description	Number	Pin Name	Description	Number
CK[1:0]	Clock Inputs, positive line	2	SA[1:0]	SPD and TS address	2
/CK[1:0]	Clock inputs, negative line	2	DQ[63:0]	Data Input/Output	64
CKE[1:0]	Clock Enables	2	DM[7:0]	Data Masks	8
/RAS	Row Address Strobe	1	DQS[7:0]	Data strobes	8
/CAS	Column Address Strobe	1	/DQS[7:0]	Data strobes complement	8
/WE	Write Enable	1	TEST	Logic Analyzer specific test pin (No connect on SO-DIMM)	1
/S[1:0]	Chip Selects	2	VDD	Core and I/O Power	12
A[9:0],A[11:15]	Address Inputs	15	VSS	Ground	57
A10,AP	Address Input/Autoprecharge	1	VREF	Input/Output Reference	1
BA[2:0]	SDRAM Bank Address	3	VDDSPD	SPD and TS Power	1
ODT[1:0]	On-die termination control	2	/Event Pin	Reserved for optional hardware temperature sensing	1
SCL	Serial Presence Detect (SPD) and Thermal sensor(TS) Clock Input	1	NC	Reserved for future use	3
SDA	SPD and TS Data Input/Output	1		**Total:**	**200**

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6. Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0 - /CK0 CK1 - /CK1	Input	Cross point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling edge of /CK. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE[1:0]	Input	Active High	Activates the DDR2 SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.
/S[1:0]	Input	Active Low	Enables the associated DDR2 SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by /S0; Rank 1 is selected by /S1.
/RAS, /CAS, /WE	Input	Active Low	When sampled at the cross point of the rising edge of CK and falling edge of CK and CAS, RAS, and WE define the operation to be executed by the SDRAM.
BA[2:0]	Input	—	Selects which DDR2 SDRAM internal bank of four or eight is activated.
ODT[1:0]	Input	Active High	Asserts on-die termination for DQ, DM, DQS, and /DQS signals if enabled via the DDR2 SDRAM mode register.
A[9:0], A10/AP, A[15:11]	Input	—	During a Bank Activate command cycle, defines the row address when sampled at the cross point of the rising edge of CK and falling edge of /CK. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of /CK. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0-BAn inputs. If AP is low, then BA0-BAn are used to define which bank to precharge.
DQ[63:0]	In/Out	—	Data Input/Output pins.
DM[7:0]	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect.

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DQS[7:0], /DQS[7:0]	In/Out	Cross point	The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode, the data strobe is sourced by the DDR2 SDRAMs and is sent at the leading edge of the data window. /DQS signals are complements, and timing is relative to the crosspoint of respective DQS and /DQS. If the module is to be operated in single ended strobe mode, all /DQS signals must be tied on the system board to VSS and DDR2 SDRAM mode registers programmed appropriately.
VDD, VDDSPD, VSS	Supply	—	Power supplies for core, I/O, Serial Presence Detect, Thermal sensor, and ground for the module.
VREF	Supply	—	Reference voltage for SSTL18 inputs.
SDA	In/Out	—	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM or Thermal sensor. A resistor must be connected from the SDA bus line to VDDSPD on the system planar to act as a pull up.
SCL	Input	—	This signal is used to clock data into and out of the SPD EEPROM and Thermal sensor.
SA[1:0]	Input	—	Address pins used to select the Serial Presence Detect base address.
TEST	In/Out	—	The TEST pin is reserved for bus analysis tools and is not connected on normal memory modules (SO-DIMMs).
/Event	Wire-OR Out	Active Low	The optional EVENT pin is reserved for use to flag critical module temperatures and is used in conjuction with a SPD temperture sensing option.

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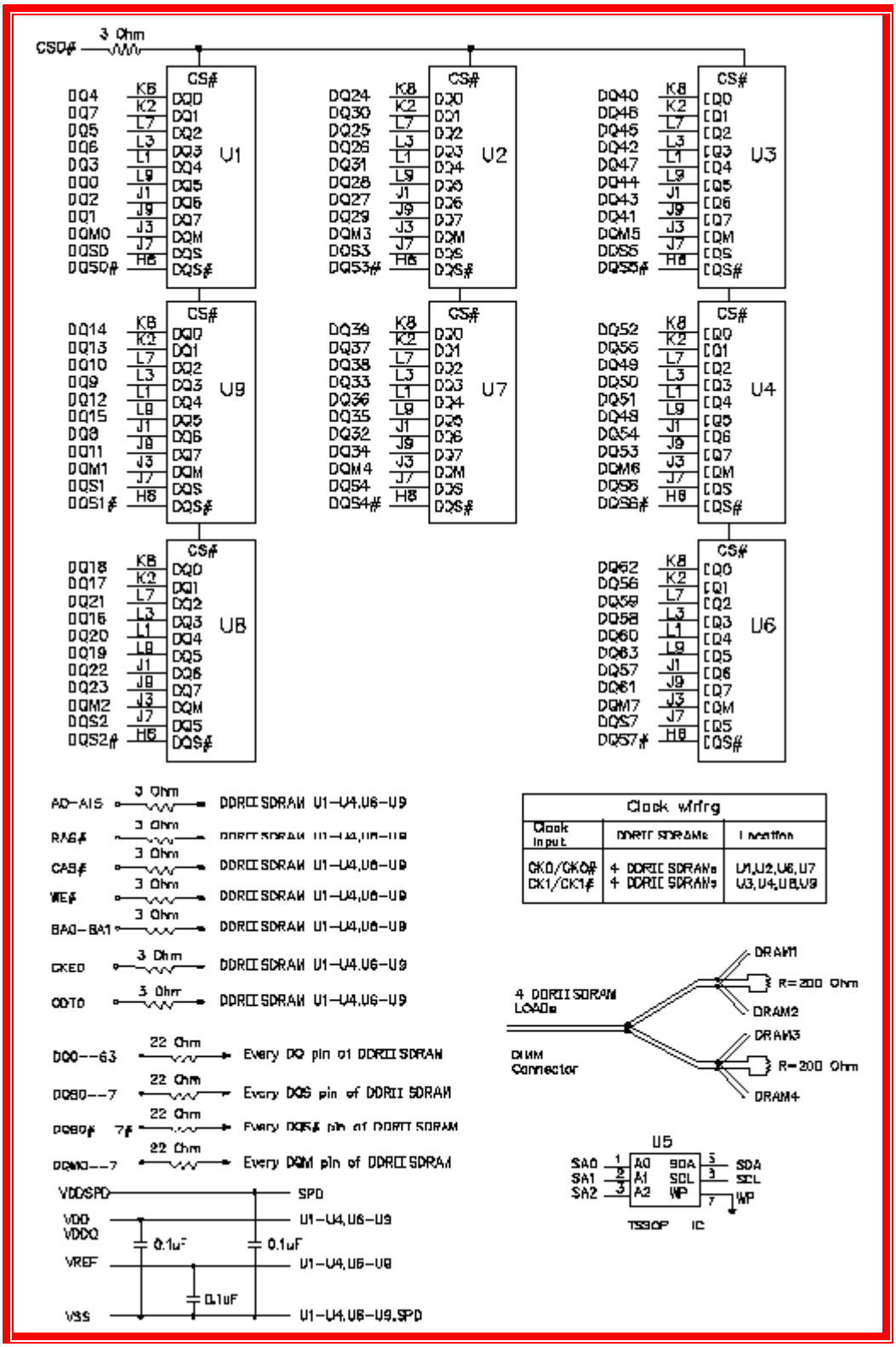
7. Function Block Diagram:

- (1 Rank, 128Mx8 DDR2 base SDRAM Module)



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8. Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	NOTE
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	-1.0V~2.3V	V	1
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	-0.5V~2.3V	V	1
V_{DDL}	Voltage on V_{DDL} pin relative to V_{SS}	-0.5V~2.3V	V	1
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.5V~2.3V	V	1

NOTE:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. V_{DD} and V_{DDQ} must be within 300mV of each other at all times; and V_{REF} must be not greater than 0.6 x V_{DDQ}. When V_{DD} and V_{DDQ} and V_{DDL} are less than 500mV, V_{REF} may be equal to or less than 300mV.
4. Voltage on any input or I/O may not exceed voltage on V_{DDQ}.

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9. AC & DC Operating Conditions

9.1 Recommended DC operating Conditions

Symbol	Parameter	Rating			Units	NOTE
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	1.7	1.8	1.9	V	
V_{DDL}	Supply Voltage for DLL	1.7	1.8	1.9	V	4
V_{DDQ}	Supply Voltage for Output	1.7	1.8	1.9	V	4
V_{REF}	Input Reference Voltage	0.49*V_{DDQ}	0.50*V_{DDQ}	0.51*V_{DDQ}	mV	1,2
V_{TT}	Termination Voltage	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V	3

NOTE : There is no specific device V_{DD} supply voltage requirement for SSTL-1.8 compliance. However under all conditions V_{DDQ} must be less than or equal to VDD.

1. The value of V_{REF} may be selected by the user to provide optimum noise margin in the system. Typically the value of V_{REF} is expected to be about 0.5 x V_{DDQ} of the transmitting device and V_{REF} is expected to track variations in V_{DDQ}.
2. Peak to peak AC noise on V_{REF} may not exceed +/-2% V_{REF}(DC).
3. V_{TT} of transmitting device must track V_{REF} of receiving device.
4. AC parameters are measured with V_{DD}, V_{DDQ} and V_{DDL} tied together.

9.2 DRAM Operating Temperature Condition

Symbol	Parameter		Rating	Units	Note
T_{OPER}	Operating Temperature Range	Normal Temperature	0 to 85	°C	1,2

Note:

1. Operating Temperature TOPER is the case surface temperature on the center/top side of the DRAM.
2. T_{CASE} > 85°C ➔ T_{REFI} = 3.9μs. All DRAM specification only support 0°C < T_{CASE} < 85°C

9.3 Input DC / AC Logic Level

Symbol	Parameter	Min.	Max.	Units	Note
V_{IH}(DC)	DC input logic high	V_{REF}+0.125	V_{DDQ}+0.3	V	
V_{IL}(DC)	DC input logic low	-0.3	V_{REF}-0.125	V	

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V_{IH}(AC)	AC input logic high	V_{REF}+0.200	-	V	1
V_{IL}(AC)	AC input logic low	-	V_{REF}-0.200	V	1

NOTE :

1. For information related to VPEAK value, Refer to overshoot/undershoot specification in device operation and timing datasheet; maximum peak amplitude allowed for overshoot and undershoot.

9.4 AC Input Test Conditions

Symbol	Condition	Value	Units	NOTE
V_{REF}	Input reference voltage	0.5*V_{DDQ}	V	1
V_{SWING}(MAX)	Input signal maximum peak to peak swing	1.0	V	1
SLEW	Input signal minimum slew rate	1.0	V/ns	2,3

NOTE:

1. Input waveform timing is referenced to the input signal crossing through the $V_{IH/IL}$(AC) level applied to the device under test.
2. The input signal minimum slew rate is to be maintained over the range from V_{REF} to V_{IH}(AC) min for rising edges and the range from V_{REF} to V_{IL}(AC) max for falling edges as shown in the below figure.
3. AC timings are referenced with input waveforms switching from V_{IL}(AC) to V_{IH}(AC) on the positive transitions and V_{IH}(AC) to V_{IL}(AC) on the negative transitions.

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10. Operating, Standby, and Refresh Currents

- 1GB SODIMM (1Rank, 128Mx8 DDR2 SDRAMs)

Symbol	Parameter/Condition	PC2-6400	Unit
I_{DD0}	Operating Current: one bank; active/precharge; tRC = tRC (MIN); tCK = tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	520	mA
I_{DD1}	Operating Current: one bank; active/read/precharge; Burst = 2; tRC = tRC (MIN); CL=2.5; tCK = tCK (MIN); IOUT = 0mA; address and control inputs changing once per clock cycle	600	mA
I_{DD2P}	Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE ≤ VIL (MAX); tCK = tCK (MIN)	80	mA
I_{DD2N}	Idle Standby Current: CS ≥ VIH (MIN); all banks idle; CKE ≥ VIH (MIN); tCK = tCK (MIN); address and control inputs changing once per clock cycle	224	mA
I_{DD2Q}	Precharge Quiet Standby Current: All banks idle; is HIGH; CKE is HIGH; $t_{CK} = t_{CK\ (MIN)}$; Other control and address inputs are stable, Data bus inputs are floating.	192	mA
I_{DD3PF}	Active Power-Down Current: All banks open; tCK = tCK (MIN), CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to **low** (Fast Power-down Exit).	240	mA
I_{DD3PS}	Active Power-Down Current: All banks open; tCK = tCK (MIN), CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to **high** (Slow Power-down Exit).	160	mA
I_{DD3N}	Active Standby Current: one bank; active/precharge; CS ≥ VIH (MIN); CKE ≥ VIH (MIN); tRC = tRAS (MAX); tCK = tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	264	mA
I_{DD4W}	Operating Current: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL=2.5; tCK = tCK (MIN)	1000	mA
I_{DD4R}	Operating Current: one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; tCK = tCK (MIN); IOUT = 0mA	960	mA
I_{DD5}	Auto-Refresh Current: tRC = tRFC (MIN)	1240	mA
I_{DD6}	Self-Refresh Current: CKE ≤ 0.2V	56	mA
I_{DD7}	Operating Current: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; tRC = tRC (min); IOUT = 0mA.	1680	mA

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11. AC Timing Specifications

Symbol	Parameter	PC2-6400		Unit
		Min.	Max.	
t_{AC}	DQ output access time from CK/CK#	-0.40	+0.40	ns
t_{DQSCK}	DQS output access time from CK/CK#	-0.35	+0.35	ns
t_{CH}	CK high-level width	0.48	0.52	t_{CK}
t_{CL}	CK low-level width	0.48	0.52	t_{CK}
t_{HP}	Minimum half clk period for any given cycle; defined by clk high (t_{CH}) or clk low (t_{CL}) time	t_{CH} or t_{CL}	-	t_{CK}
t_{CK}	Clock Cycle Time	2.5	8	ns
t_{DS}	DQ and DM input setup time(differential data strobe)	0.05	-	ns
t_{DH}	DQ and DM input hold time(differential data strobe)	0.125	-	ns
t_{IPW}	Input pulse width	0.6	-	t_{CK}
t_{DIPW}	DQ and DM input pulse width (each input)	0.35	-	t_{CK}
t_{HZ}	Data-out high-impedance time from CK/XK	-	t_{ACmax}	ns
$t_{LZ(DQS)}$	DQS low-impedance time from CK/XK	t_{ACmin}	t_{ACmax}	ns
$t_{LZ(DQ)}$	DQ low-impedance time from CK/XK	$2*t_{AC}$ min	t_{AC} max	ns
t_{DQSQ}	DQS-DQ skew (DQS & associated DQ signals)	-	0.20	ns
t_{QHS}	Data hold Skew Factor	-	0.30	ns
t_{QH}	Data output hold time from DQS	t_{HP} - t_{QHS}	-	ns
t_{DQSS}	Write command to 1st DQS latching transition	-0.25	+0.25	t_{CK}
$t_{DQSL,(H)}$	DQS input low (high) pulse width (write cycle)	0.35	-	t_{CK}
t_{DSS}	DQS falling edge to CK setup time (write cycle)	0.2	-	t_{CK}
t_{DSH}	DQS falling edge hold time from CK (write cycle)	0.2	-	t_{CK}
t_{MRD}	Mode register set command cycle time	2	-	t_{CK}
t_{WPST}	Write postamble	0.40	0.60	t_{CK}

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t_{WPRE}	Write preamble	0.35	-	t_{CK}
t_{IH}	Address and control input hold time	250	-	Ps
t_{IS}	Address and control input setup time	175	-	Ps
t_{RPRE}	Read preamble	0.90	1.10	t_{CK}
t_{RPST}	Read postamble	0.40	0.60	t_{CK}
t_{RRD}	Active bank A to Active bank B command	7.5	-	Ns
tDelay	Minimum time clocks remains ON after CKE asynchronously drops Low	$t_{IS} + t_{CK} + t_{IH}$	-	Ns
t_{REFI}	Average Periodic Refresh Interval ($85^oC < T_{CASE} \leq 95^oC$)	3.9		Ms
	Average Periodic Refresh Interval ($0^oC \leq T_{CASE} \leq 85^oC$)	7.8		Ms
t_{OIT}	OCD drive mode output delay	0	12	Ns
t_{CCD}	CAS# to CAS# delay	2		t_{CK}
t_{WR}	Write recovery time without Auto-Precharge	15	-	Ns
t_{DAL}	Auto precharge write recovery + precharge time	$WR+t_{RP}$	-	t_{CK}
t_{WTR}	Internal write to read command delay	7.5	-	Ns
t_{RTP}	Internal read to precharge command delay	7.5		Ns
t_{XSNR}	Exit self refresh to a Non-read command	$t_{RFC}+10$		Ns
t_{XSRD}	Exit self refresh to a Read command	200		t_{CK}
t_{XP}	Exit precharge power down to any Non- read command	2	-	t_{CK}
t_{XARD}	Exit active power down to read command	2	-	t_{CK}
t_{XARDS}	Exit active power down to read command	8-AL		t_{CK}
t_{CKE}	CKE minimum pulse width	3		t_{CK}
t_{AOND}	ODT turn-on delay	2	2	t_{CK}
t_{AON}	ODT turn-on	$t_{AC\ (min)}$	$t_{AC\ (max)}$ +0.7	Ns
t_{AONPD}	ODT turn-on (Power down mode)	$t_{AC\ (min)}$ +2	$2t_{CK}$ + $t_{AC(max)}$ +1	Ns

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t_{AOFD}	ODT turn-off delay	2.5	2.5	t_{CK}
t_{AOF}	ODT turn-off	$t_{AC(min)}$	$t_{AC(max)}$ +0.6	Ns
t_{AOFPD}	ODT turn-off (Power down mode)	$t_{AC\ (min)}$+2	2.5t_{CK} + $t_{AC(max)}$ +1	Ns
t_{ANPD}	ODT to power down entry latency	3		t_{CK}
t_{AXPD}	ODT power down exit latency	8		t_{CK}

12. Speed Grade Definition

Symbol	Parameter	PC2-6400		Unit
		Min	Max	
t_{RAS}	Row Active Time	45	70,000	ns
t_{RC}	Row Cycle Time	60	-	ns
t_{RCD}	RAS to CAS delay	15	-	ns
t_{RP}	Row Precharge Time	15	-	ns

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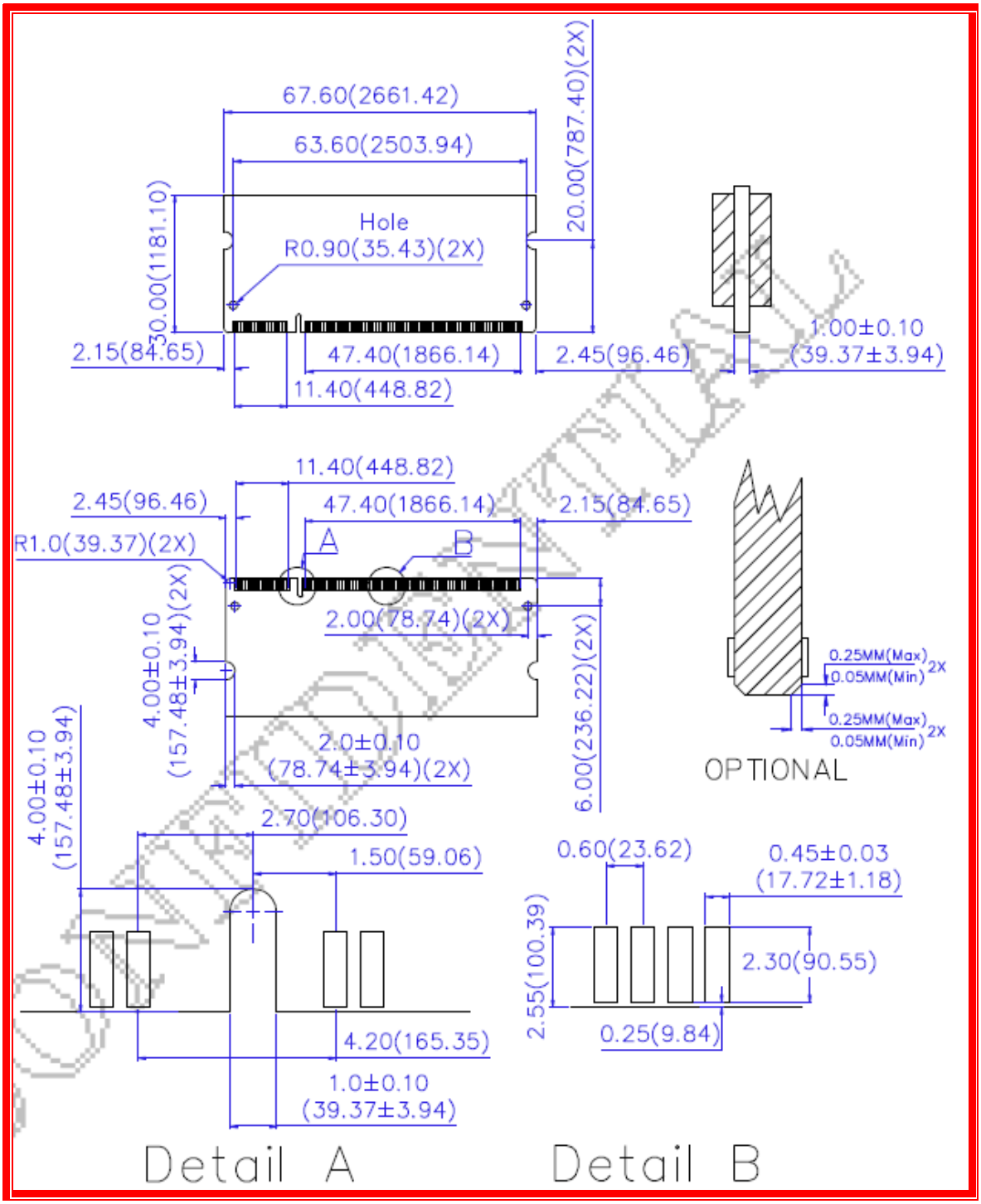
13. Physical Dimension



Note: All dimensions are in millimeters (mils) and should be kept within a tolerance of ±0.15 (6), unless otherwise specified.

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14. RoHS Declaration

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宜鼎國際股份有限公司
Innodisk Corporation

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RoHS 自我宣告書 (RoHS Declaration of Conformity)

Manufacturer Product: All Innodisk EM Flash and Dram products

一、 宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟 2011/65/EU 及(EU) 2015/863 關於 RoHS 之規範要求。

Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) and (EU) 2015/863 requirement.

二、 本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。

Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.

Name of hazardous substance	Limited of RoHS ppm (mg/kg)
鉛 (Pb)	< 1000 ppm
汞 (Hg)	< 1000 ppm
鎘 (Cd)	< 100 ppm
六價鉻 (Cr 6+)	< 1000 ppm
多溴聯苯 (PBBs)	< 1000 ppm
多溴二苯醚 (PBDEs)	< 1000 ppm
鄰苯二甲酸二(2-乙基己基)酯 (DEHP)	< 1000 ppm
鄰苯二甲酸丁酯苯甲酯 (BBP)	< 1000 ppm
鄰苯二甲酸二丁酯 (DBP)	< 1000 ppm
鄰苯二甲酸二異丁酯 (DIBP)	< 1000 ppm

立 保 證 書 人 (Guarantor)

Company name 公司名稱： Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人： Randy Chien 簡川勝

Company Representative Title 公司代表人職稱： Chairman 董事長

Date 日期： 2017 / 01 / 18

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Revision Log

Rev	Date	Modification
0.1	9th January 2018	Preliminary Edition
1.0	9th January 2018	Official Release
1.1	11st January 2018	Modified typo for timing of 1.feature and 12. Speed Grade Definition
1.2	26th September 2018	Revised 4.Pin Configurations

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