HSP051-4M5

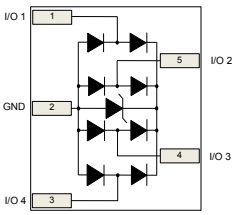
Datasheet

4-line ESD protection for high speed





µQFN-5L



Product status link
HSP051-4M5

Features

- Very compact 500 µm pitch package, for easy PCB layout
- Very-large bandwidth: 11.5 GHz
- Very-low capacitance: 0.2 pF (I/O to I/O) and 0.35 pF (I/O to GND)
- Very low dynamic resistance : 0.35 Ω
- Low leakage current: < 1 nA
- High ESD protection level
- High integration
- Suitable for high density boards
- Extended operating junction temperature range : -40 °C to 150 °C
- Exceeds IEC 61400-4-2 level standard:
  - ±20 kV (contact discharge)
  - ±30 kV (air discharge)

Applications

The HSP051-4M5 is designed to protect against to electro-static discharge sub-micron technology circuits driving:

- HDMI 2.1, HDMI 2.0 and HDMI 1.4
- USB 3.1 Gen 1 and Gen 2
- Display port
- Digital video interface
- Serial ATA

The ultra-low variation of the capacitance ensures very low influence on signal-skew. The large bandwidth make it compatible with HDMI 2.1 8K (12 Gbps), HDMI 2.0 4K/2K (5.94 Gbps) and USB 3.1 Gen 2 (10 Gbps).

Description

The HSP051-4M5 is a 4-channel ESD array with a rail to rail architecture designed specifically for the protection of high speed differential lines.

The device is packaged in µQFN 1.3 mm x 0.8 mm with a 500 µm pitch.

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage	IEC 61000-4-2: Contact discharge Air discharge	 20 30	kV
I_{PP}	Peak pulse current (8/20 µs)		3	A
T_{stg}	Storage temperature range		-65 to +150	°C
T_j	Operating junction temperature range		-40 to +150	
T_L	Maximum lead temperature for soldering during 10 s		260	

Figure 1. Electrical characteristics - parameters definition

Symbol		Parameter
V_{BR}	=	Breakdown voltage
V_{CL}	=	Clamping voltage
I_{RM}	=	Leakage current at V_{RM}
V_{RM}	=	Stand-off voltage
I_F	=	Forward current
I_R	=	Breakdown current
I_{PP}	=	Peak pulse current
V_F	=	Forward voltage drop
R_d	=	Dynamic resistance

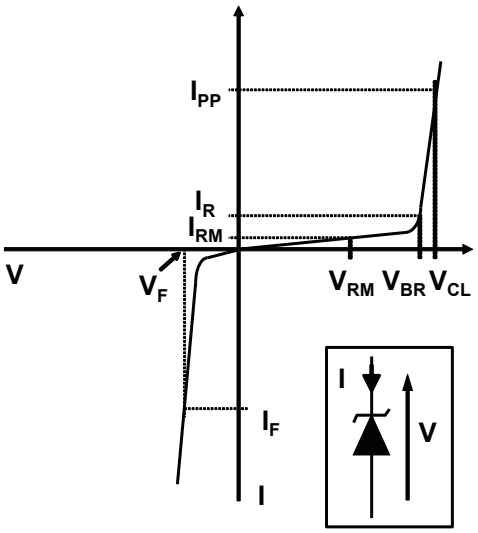


Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	Breakdown voltage		I_R = 1 mA	5.7	6.4		V
V_{RM}	Reverse working voltage					5	
I_{RM}	Leakage current		V_{RM} = 3.6 V per line		< 1	50	nA
			V_{RM} = 5 V per line		3	70	
V_{CL}	Reverse Clamping voltage		I_{pp} = 3A, 8/20µs			11.3	V
			TLP measurement (pulse duration 100 ns), 16 A I_{pp}		13.7		
			8 kV contact discharge after 30 ns, IEC 61000-4-2		13		
R_d	Dynamic resistance, TLP measurement (pulse duration 100 ns)		I/O to GND		0.35		Ω
			GND to I/O		0.45		
$C_{I/O - I/O}$	Capacitance	$V_{I/O}$ = 0 V, V_{OSC} = 30 mV	F = 2.5 GHZ to 9 GHz		0.20	0.30	pF
$C_{I/O - GND}$			F = 200 MHZ to 2.5 GHz		0.60	0.76	
			F = 2.5 GHZ to 9 GHz		0.35	0.43	
f_C	Differential mode cut-off frequency at - 3dB				11.50		GHz

1.1 Characteristics (curves)

Figure 2. Leakage current versus junction temperature (typical values)

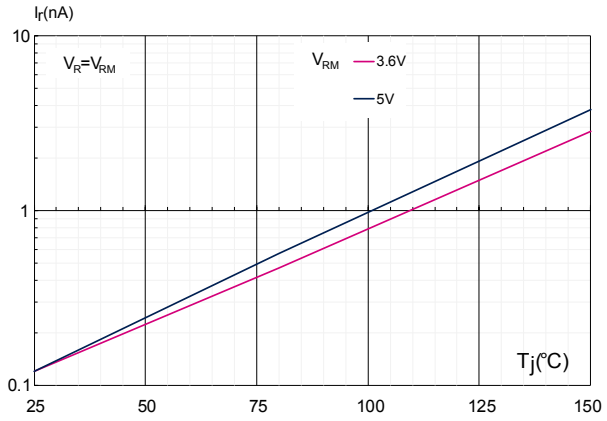


Figure 3. S21 attenuation measurement

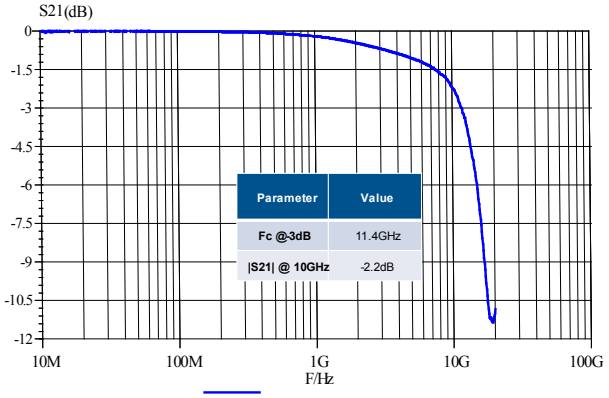


Figure 4. HDMI2.1 12 Gbps eye diagram without HSP051-4M5 (with worst cable model (WCM3), EQ with 8 dB CTLE and One-tap DFE



Figure 5. HDMI2.1 12 Gbps eye diagram with HSP051-4M5 (with worst cable model (WCM3), EQ with 8 dB CTLE and One-tap DFE

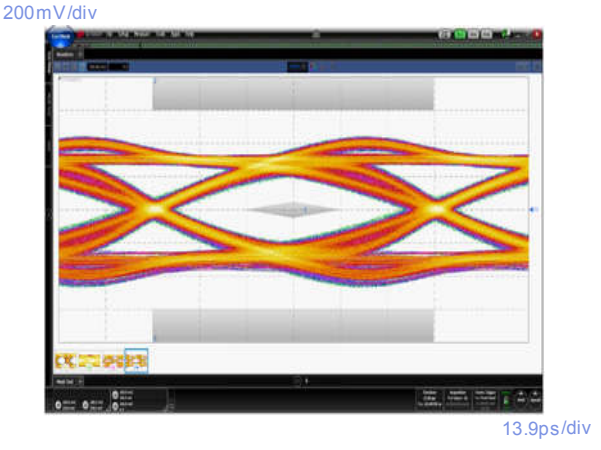


Figure 6. HDMI2.0 5.94 Gbps eye diagram without HSP051-4M5 (with worst cable model and equalizer)

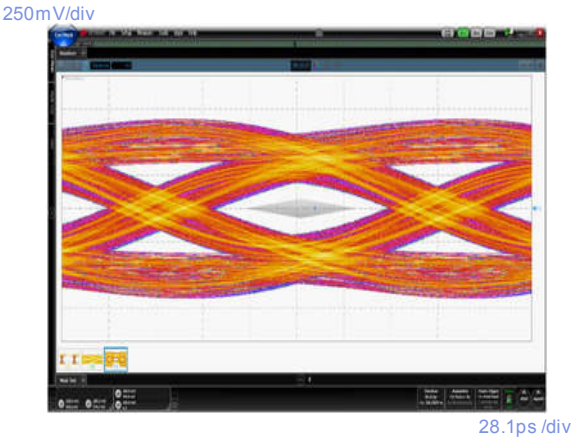


Figure 7. HDMI2.0 5.94 Gbps eye diagram with HSP051-4M5 (with worst cable model and equalizer)

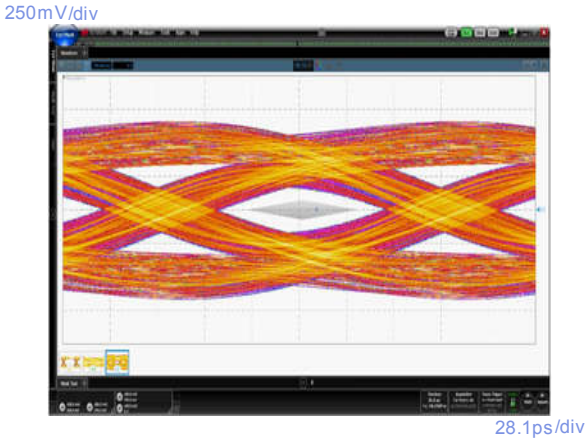


Figure 8. USB3.1 Gen 2 10.0 Gbps eye diagram without HSP051-4M5 (with type C connector, reference cable, equalizer with ADC = 6 dB and DFE)

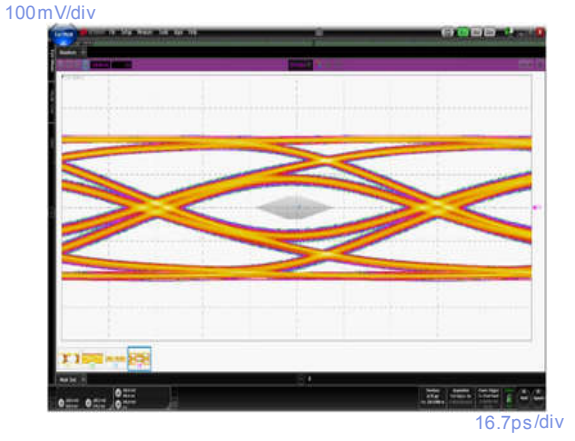


Figure 9. USB3.1 Gen 2 10.0 Gbps eye diagram with HSP051-4M5 (with type C connector, reference cable, equalizer with ADC = 6 dB and DFE)

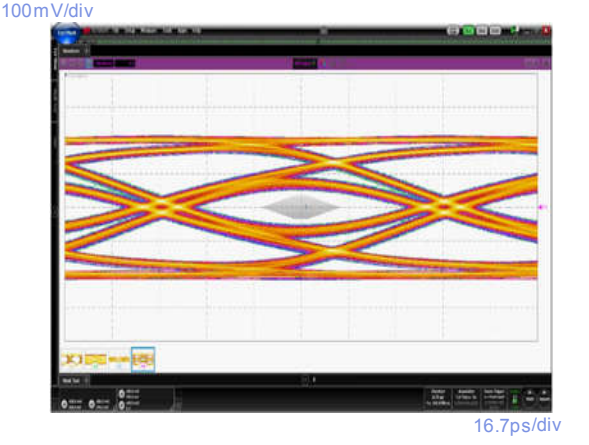


Figure 10. USB3.1 Gen 1 5.0 Gbps eye diagram without HSP051-4M5 (with type C connector, reference cable and equalizer)

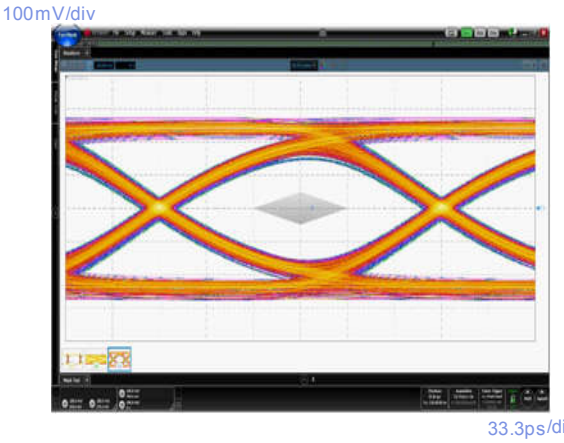


Figure 11. USB3.1 Gen 2 10.0 Gbps eye diagram with HSP051-4M5 (with type C connector, reference cable and equalizer)

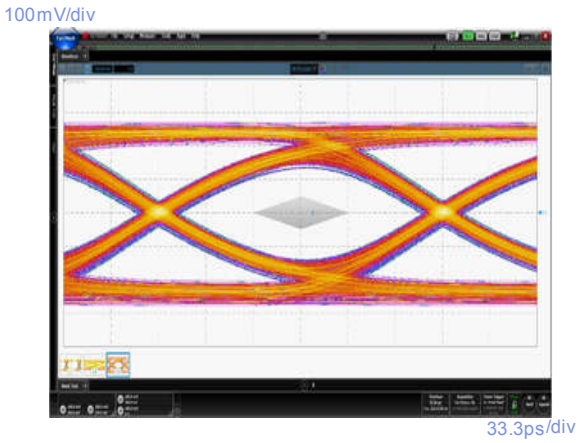
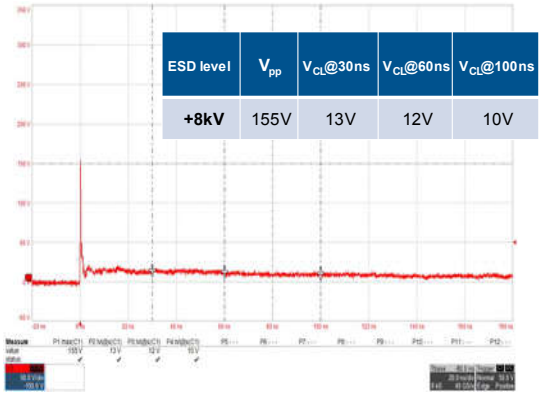
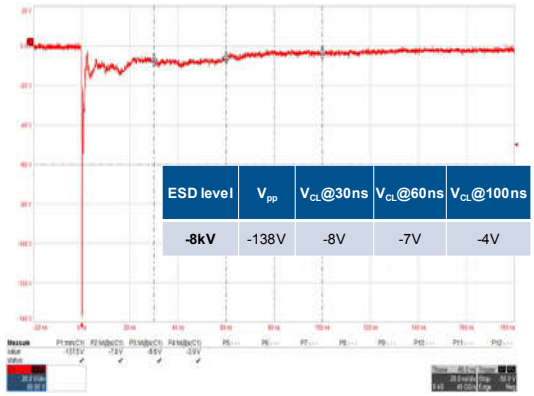


Figure 12. ESD response to IEC61000-4-2 (+8 kV contact discharge)



ESD level	V_{pp}	V_{CL}@30ns	V_{CL}@60ns	V_{CL}@100ns
+8kV	155V	13V	12V	10V

Figure 13. ESD response to IEC61000-4-2 (-8 kV contact discharge)



ESD level	V_{pp}	V_{CL}@30ns	V_{CL}@60ns	V_{CL}@100ns
-8kV	-138V	-8V	-7V	-4V

Figure 14. TLP Characteristic (pulse duration 100 ns)

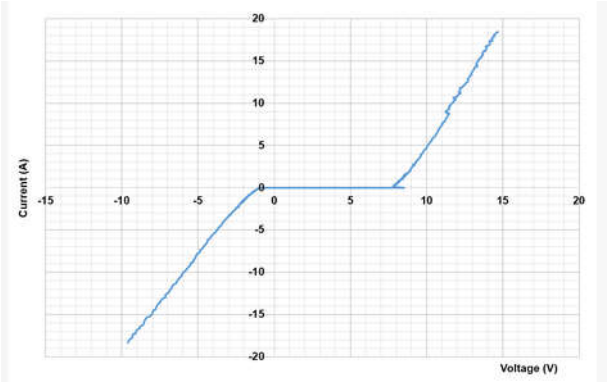
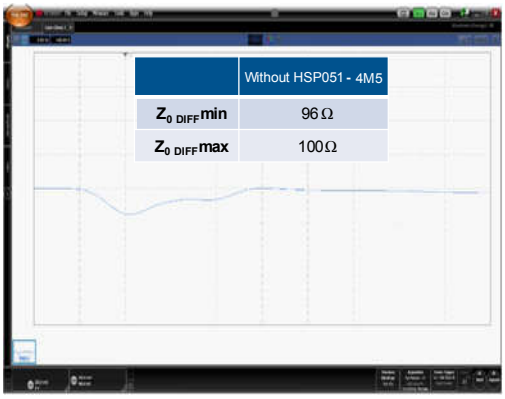


Figure 15. TDR measurement without HSP051-4M5

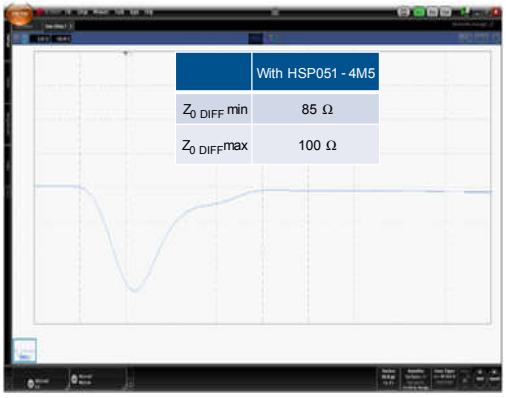
5Ω/div



200ps/div

Figure 16. TDR measurement with HSP051-4M5

5Ω/div



200ps/div

2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

2.1 MicroQFN-5L package information

Figure 17. MicroQFN-5L package outline

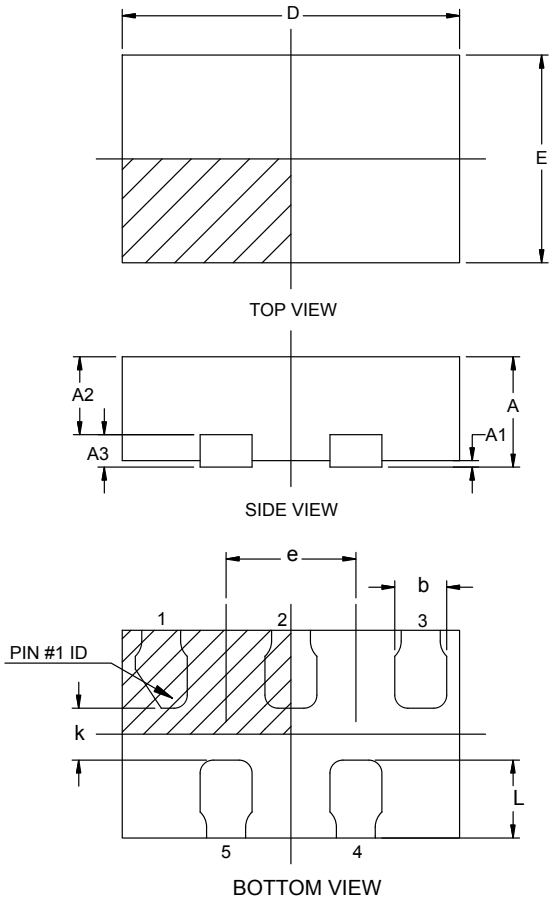


Table 3. **MicroQFN-5L package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.31	0.38	0.40	0.012	0.015	0.016
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.15	0.25	0.35	0.005	0.010	0.014
A3		0.130			0.005	
b	0.15	0.20	0.25	0.005	0.008	0.010
D	1.20	1.30	1.40	0.047	0.051	0.056
e		0.50			0.020	
E	0.70	0.80	0.90	0.027	0.031	0.036
L	0.20	0.25	0.30	0.007	0.010	0.012
k	0.20	0.25		0.007	0.010	

Figure 18. **Footprint (dimensions in mm)**

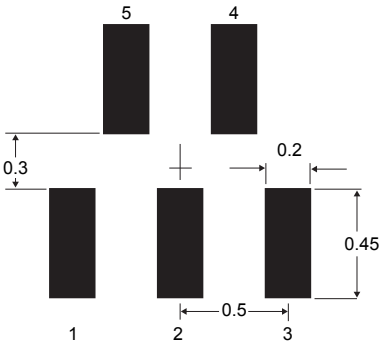


Figure 19. **Marking**

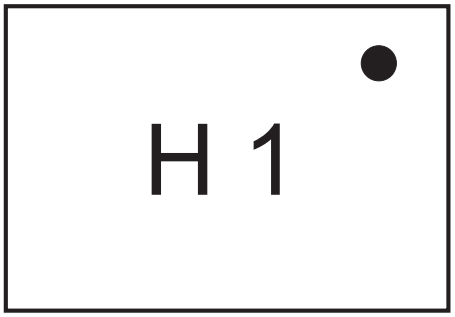
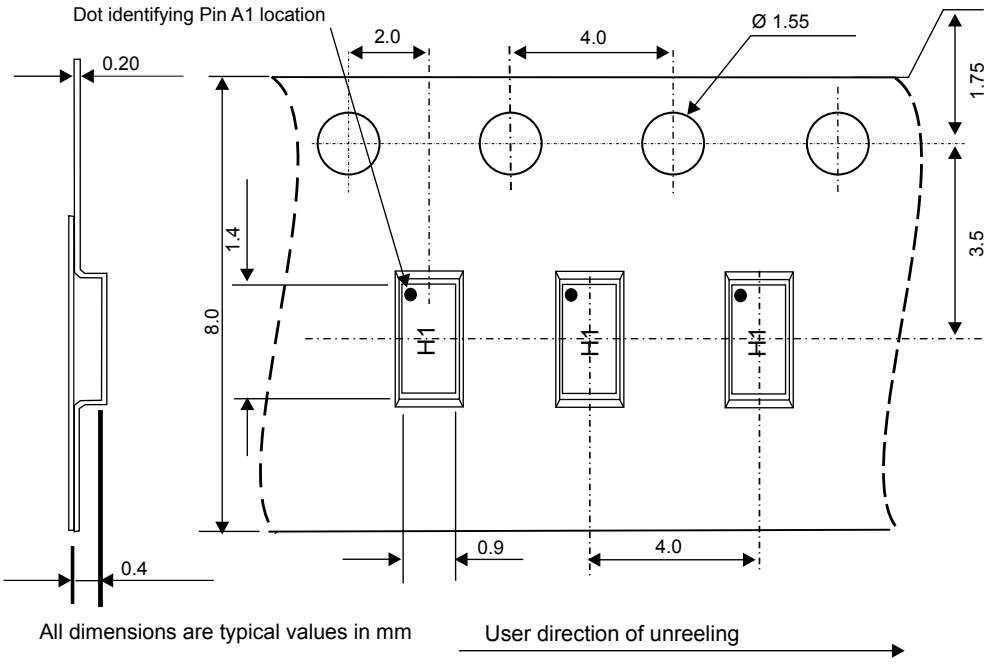


Figure 20. **Tape and reel specification**



3 Recommendation on PCB assembly

3.1 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Solder paste with fine particles: powder particle size is 20-45 µm.

3.2 Placement

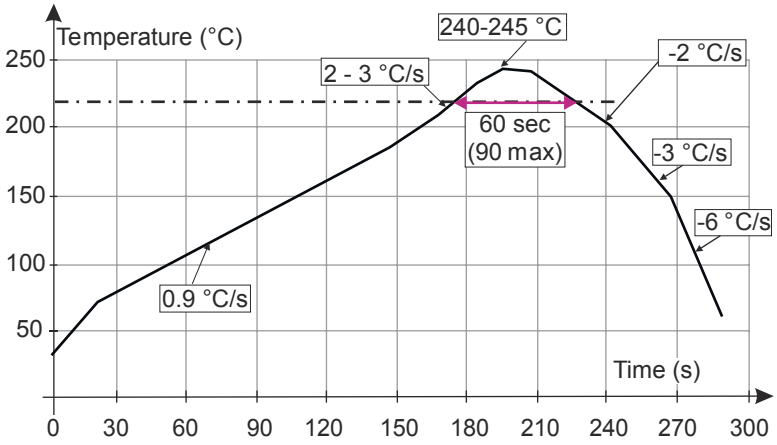
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ±0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.3 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

3.4 Reflow profile

Figure 21. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

Note: Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

4 Ordering information

Figure 22. **Ordering information scheme**

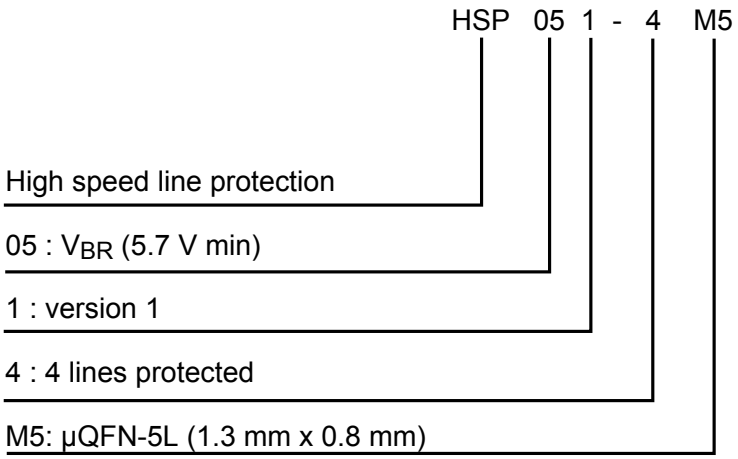


Table 4. **Ordering information**

Order code	Marking[1]	Package	Weight	Base qty.	Delivery mode
HSP051-4M5	H1	µQFN-5L	1.04 mg	6000	Tape and reel

1. *The marking can be rotated by multiples of 90° to differentiate assembly location*

Revision history

Table 5. **Document revision history**

Date	Revision	Changes
04-Feb-2016	1	Initial release.
21-Dec-2018	2	New version of product.
07-Feb-2019	3	Updated link syntax.

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