Simple design with built-in self-controlled cell balance features circuit

Cell Balance LSI of 4 to 6 Series Power Storage Element Cells for Automotive

BD14000EFV-C

General Description

BD14000EFV is a LSI IC designed as a self-controlled cell balancer. It has a built-in shunt-type power storage element balancer function that can respond to 4 to 6 cells. All the functions necessary in a cell balancer are built-in making power storage element cell balancing possible only in this LSI.

This chip can be used for electric double layer capacitors (EDLC) with cell detection voltage range of 2.4V to 3.1V and power storage capacitors which is important for cell balancers with similar electrical characteristics

It has a built-in multiple over-voltage detection function and can also detect abnormal mode such as any characteristic deterioration in cells.

Also, application-dependent operation can be set since enable control is possible.

Features

- AEC-Q100 qualified(Note1)
- All EDLC cell balancer functions are integrated on a single chip
- Self- controlled EDLC balance function
- Adopts shunt resistance method for simple balancing
- 4 to 6 cell series connection ready
- Multiple chip series connection is possible
- Built-in over-voltage detection flag output
- Detection voltage can be set

(Note1 : Grade2)

Applications

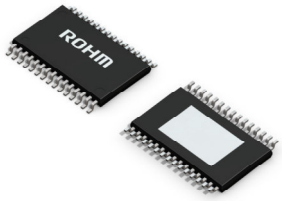
- Renewable energy power storage for Automotive, Production machinery, Building machinery, etc.
- UPS and other devices that stabilizes power supplies

Key Specifications

- Input Voltage Range : 8.0V to 24.0V
- Cell Voltage Detection Range : 2.4V to 3.1V
- Cell Voltage Detection Accuracy : ±1%(Max. at 25°C)
- Shunt Switch ON Resistance : 1Ω(Typ.)
- Operating Temp. Range : -40°C to +105°C

Package

	W (Typ) x D (Typ) x H (Max)
HTSSOP-B30	10.00mm x 7.60mm x 1.00mm



HTSSOP-B30

Typical Application Circuit

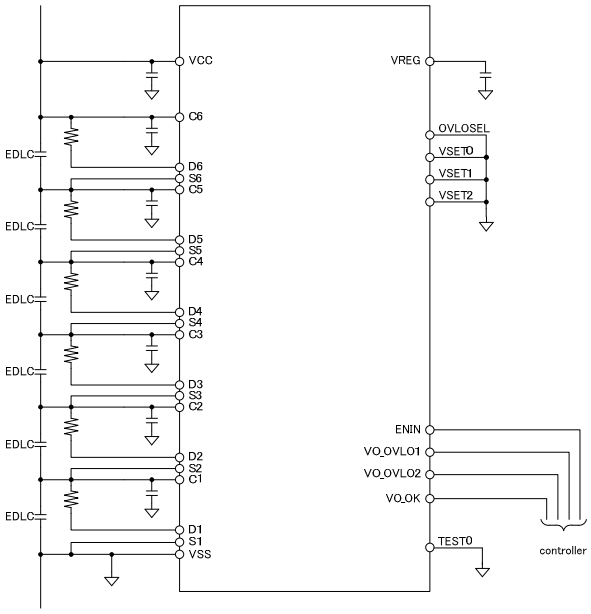


Figure 1 Typical application circuit

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

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Pin Configuration

(TOP VIEW)

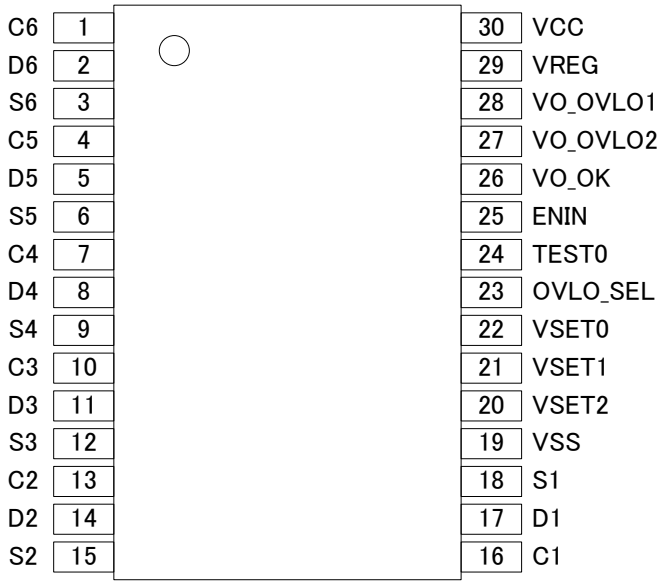


Figure 2 Pin Configuration

Pin Description

PIN No.	Symbol	Function
1	C6	Positive (+) connection terminal pin of cell 6
2	D6	Shunt switch connection terminal pin for cell 6.
3	S6	Shunt switch connection terminal pin for cell 6.
4	C5	Positive (+) connection terminal pin of cell 5
5	D5	Shunt switch connection terminal pin for cell 5.
6	S5	Shunt switch connection terminal pin for cell 5.
7	C4	Positive (+) connection terminal pin of cell 4.
8	D4	Shunt switch connection terminal pin for cell 4.
9	S4	Shunt switch connection terminal pin for cell 4.
10	C3	Positive (+) connection terminal pin of cell 3.
11	D3	Shunt switch connection terminal pin for cell 3.
12	S3	Shunt switch connection terminal pin for cell 3.
13	C2	Positive (+) connection terminal pin of cell 2
14	D2	Shunt switch connection terminal pin for cell 2.
15	S2	Shunt switch connection terminal pin for cell 2.

PIN No.	Symbol	Function
16	C1	Positive (+) connection terminal pin of cell 1
17	D1	Shunt switch connection terminal pin for cell 1
18	S1	Shunt switch connection terminal pin for cell 1
19	VSS	Analog ground (connect to (-) side of bottom cell)
20	VSET2	Detection voltage setting input pin 2
21	VSET1	Detection voltage setting input pin 1
22	VSET0	Detection voltage setting input pin 0
23	OVLOSEL	Over-voltage detection setting input pin
24	TEST0	TEST terminal pin (connect to VSS)
25	ENIN	Enable signal input pin
26	VO_OK	Self-Check OK signal output pin
27	VO_OVLO2	Overvoltage flag output pin 2
28	VO_OVLO1	Overvoltage flag output pin 1
29	VREG	Regulator circuit output pin (output capacitor : 1.0μF)
30	VCC	Regulator circuit power input pin

∗The back PAD is used for enhancing the radiation of heat. This PAD is needed to connect VSS.
∗TEST0 : This pin is used for ROHM internal test. This pin is needed to connect VSS for normal operation.

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Block Diagram

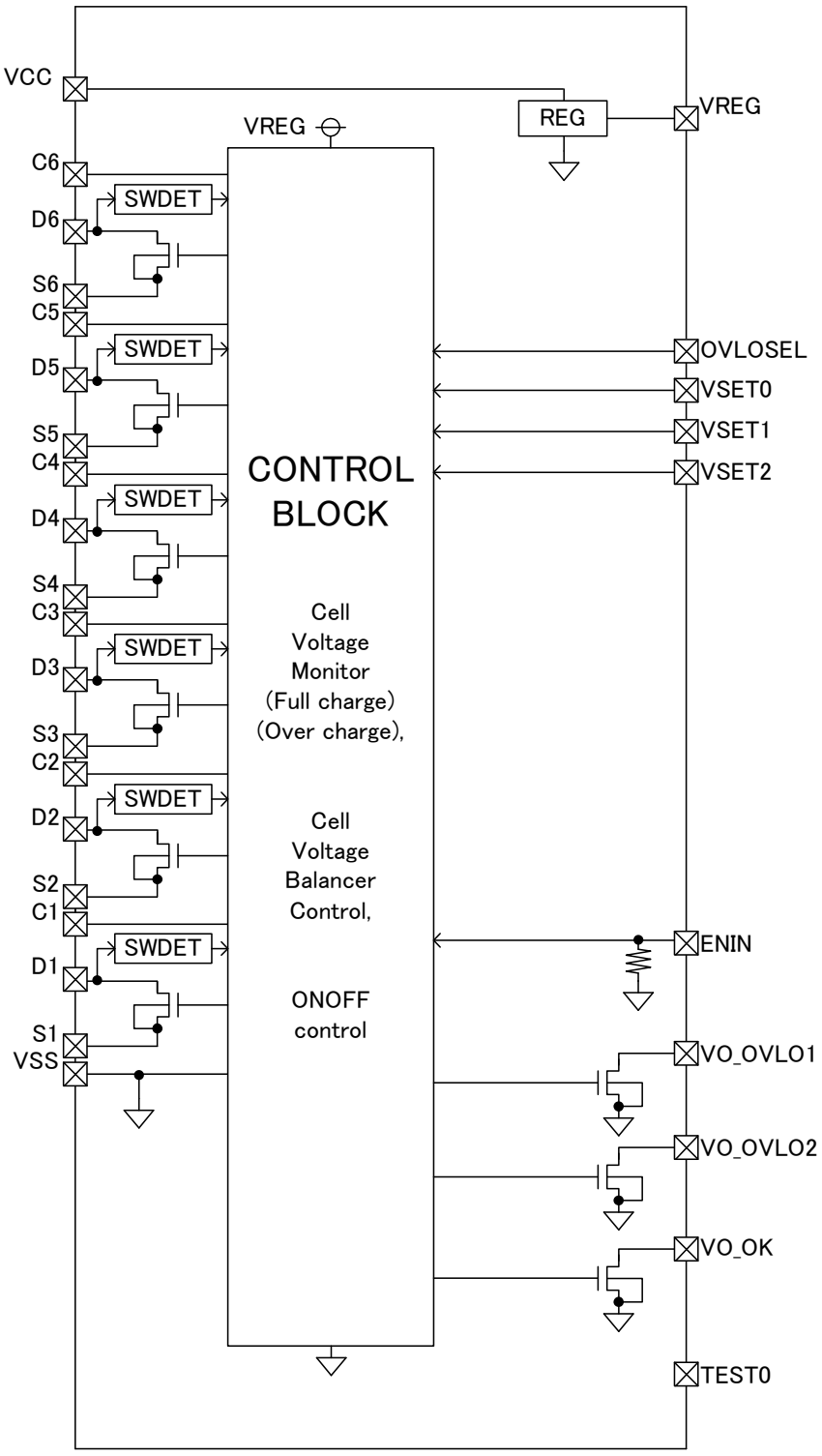


Figure 3 Block Diagram

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Description of Blocks

① CONTROL block

1. Cell voltage detection block
Setting the detection voltage is possible with cell balance voltage detection and two types of OVLO available for each cell.
Additionally, protection detection error can be controlled by setting delays for each voltage detection.

2. Detect control block
ON/OFF control is possible by setting the ENIN pin.
Additionally, cell detection voltages can be set via VSET0, 1, 2 and OVLOSEL pins.

② REG block
This is used as a power block for the chip's internal blocks.
This block can also be used as I/F power source of control input/output.

③ Shunt SW
Shunt Switch is used for the cell balancing function.

④ SWDET
SWDET detects if the drain pins (D1~D6) are normally changed to "L" when cell balance voltage is detected as a self-check function

⑤ Flag output
2 types of OVLO are output from VO_OVLO1, 2. Self-check function is output from VO_OK.

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit
Supply Voltage VCC,VCn(n=6) to VSS	V1-1	-0.3 to 28	V
Supply Voltage VCn to Vcn-1(n=2~6) VC1 to VSS VDn to Vsn (n=1~6)	V2-1	-0.3 to 7	V
Supply Voltage VREG,ENIN,VO_OVLO1,VO_OVLO2, VO_OK,OVLOSEL,VSET0,VSET1, VSET2,TEST0 to VSS	V2-2	-0.3 to 7	V
Power Dissipation	Pd	1.55 *1	W
Operating Temperature Range	Topr	-40 to +105	°C
Storage Temperature Range	Tstg	-55 to 150	°C

*1 This value is for ROHM standard board (1 layer 70x70x1.6mm) mounting. For temperatures above 25°C, use a 12.4mW/°C derating factor.
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in cases where the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta= -40°C to +105°C)

Parameter	Symbol	Rating	Unit
VCC Voltage	VCC	8.0 to 24	V

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Electrical Characteristics (Unless otherwise specified VCC=15V Ta=25°C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Circuit Current						
VCC circuit current when ON	IVCC		40	80	μA	ENIN=H During cell balance start voltage non-detection
VCC circuit current when standby	ON		25	50	μA	ENIN=L
Cn(n=1~6) pin circuit current when ON	IVCC		20	40	μA	ENIN=H,Vcn-Vcn-1=2.5V During cell balance start voltage non-detection
Cn(n=5,6) pin circuit current when standby	ICN OFF56	-	1	8	μA	ENIN=L, Vcn-Vcn-1=2.5V
Cn(n=1~4) pin circuit current when standby	OFF	-	0	5	μA	ENIN=H,Vcn-Vcn-1=2.5V
Cell Voltage Detection						
Cell Balance Start Detection Voltage Range	VCB	2.4	—	3.1	V	Set by VSET0～2 pin
Cell Balance Start Detection Accuracy1	VCB ERR1	—	—	±1	%	
Cell Balance Start Detection Accuracy2	VCB ERR2	—	—	±2	%	Ta=-40～105°C
Over- Voltage Detection 1 Detection Voltage1	VOVLO 1-1	—	VCB +0.15	—	V	Set by VSET0～2 pin and OVLOSEL=L
Over- Voltage Detection 1 Detection Voltage2	VOVLO 1-2	—	VCB +0.25	—	V	Set by VSET0～2 pin and OVLOSEL=H
Over- Voltage Detection 1 Detection Accuracy	VOVLO1 ERR	—	—	±2	%	Ta=-40～105°C
Over- Voltage Detection 2 Detection Voltage1	VOVLO2 -1	—	VCB +0.3	—	V	Set by VSET0～2 pin and OVLOSEL=L
Over- Voltage Detection 2 Detection Voltage2	VOVLO2 -2	—	VCB +0.5	—	V	Set by VSET0～2 pin and OVLOSEL=H
Over- Voltage Detection 2 Detection Accuracy	VOVLO2 ERR	—	—	±2	%	Ta=-40～105°C
Built-in Oscillator Frequency	fosc	20	40	80	kHz	
VREG						
Output Voltage	VREG	3.6	4.3	5.0	V	Io=10mA

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Electrical Characteristics (Unless otherwise specified VCC=15V Ta=25°C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Shunt SW						
Switch on resistance In between Dn-Sn (n=1~6)	Ronsw	—	1.0	2.0	Ω	Vcn-Vcn-1=2.5V
Leak current during switch off in between Dn-Sn (n=1~6)	ILEAIOW	—	—	2	μA	Vdn-Vsn-1=3.5V
Digital Input/ Output Terminal						
Output L Level Voltage (VO_OVLO1.2,VO_OK)	VOL OVLO	—	0.2	0.5	V	IIN=5mA
Leak Current when off (VO_OVLO1.2,VO_OK)	ILFAK OVLO	—	—	2	μA	VIN=3.5V
Input H Level Voltage (ENIN)	VIHEN	1.8	—	VREG +0.2	V	
Input L Level Voltage (ENIN)	VILEN	-0.3	—	0.4	V	
Input current when H level input. (ENIN)	IIHEN	—	3.5	7.0	μA	VIN=3.5V
Input H Level Voltage (VSET0～2,OVLOSEL)	VIH SET	VREG X0.8	—	VREG +0.2	V	
Input L Level Voltage (VSET0～2,OVLOSEL)	VIL SET	-0.3	—	VREG X0.2	V	
Input current when H level input (VSET0～2,OVLOSEL)	IIH SET	—	—	2	μA	VIN=3.5V
Output current when L level input (VSET0～2,OVLOSEL)	IIL SET	—	—	2	μA	VIN=0.0V

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Typical Performance Curves

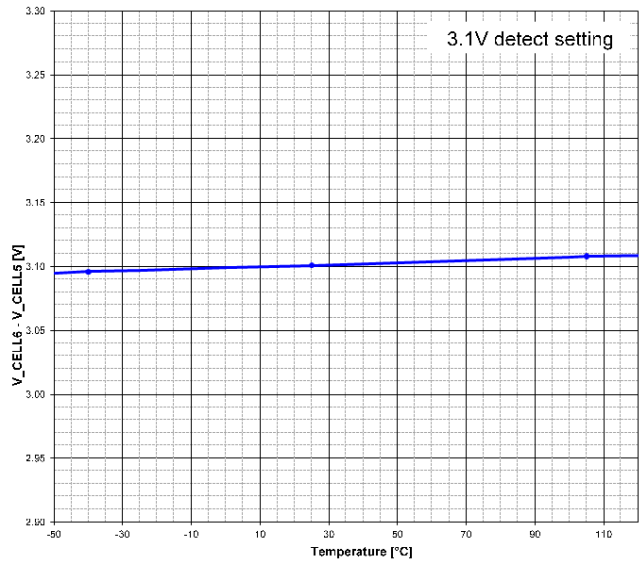


Figure 4. Detection voltage for cell balance vs. Temp.
(Detection voltage setting= 3.10V)

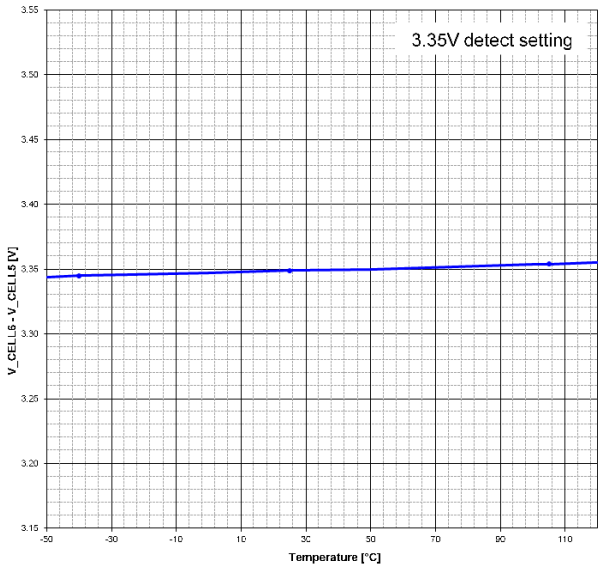


Figure 5. Detection voltage for OVLO1 vs. Temp.
(Detection voltage=3.35V setting)

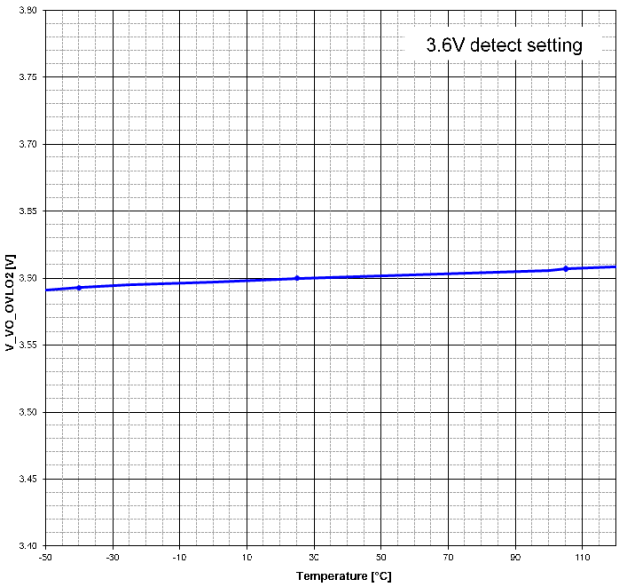


Figure 6. OVLO2 detection voltage vs. Temp.
(Detection voltage=3.60V setting)

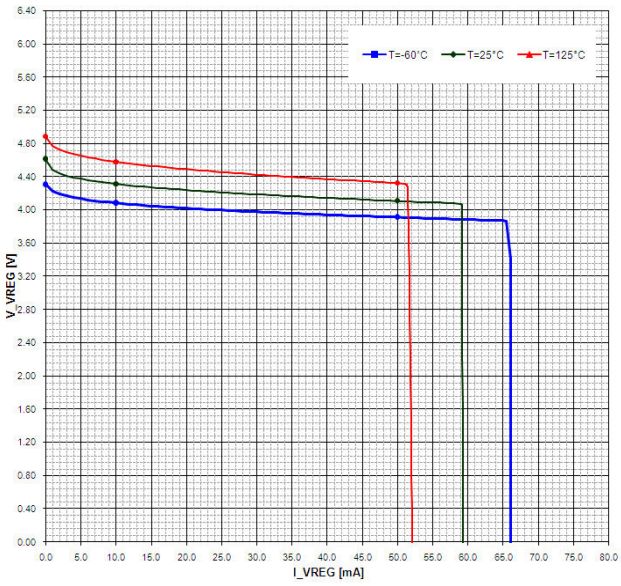


Figure 7. VREG vs IO
(VCC=15V)

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Function description and items that need attention

1. Setting the operation mode from the Enable terminal
   It is possible to control the cell balancer function ON/OFF setting of the IC via the operation mode setting pin (ENIN)
   The settings for each input terminal is shown on the following table

Input	Balancer Setting	Remarks
ENIN	ON/OFF	
0	OFF	Standby
1	ON	Operating

When standby, only the internal power supply (VREG) is operational.
When operating, the other blocks are also operational.

2. Detection Voltage Setting
   By using the detection voltage setting terminal pins (VSET0,1 and 2), setting the cell balance start detection voltage (VCB) and over-voltage detection voltage 1,2 (VOVLO1,2) is possible. Output for each input terminal is shown on the following table:

Input			Output		
VSET2	VSET1	VSET0	VCB[V]	VOVLO1[V]	VOVLO2[V]
0	0	0	2.4	VCB+0.15(*1) or VCB+0.25(*2)	VCB+0.3(*1) or VCB+0.5(*2)
0	0	1	2.5		
0	1	0	2.6		
0	1	1	2.7		
1	0	0	2.8		
1	0	1	2.9		
1	1	0	3.0		
1	1	1	3.1		

(*1) : OVLOSEL='L' condition
(*2) : OVLOSEL='H' condition

3. Over-Voltage Flag output
   The Over- Voltage Detection Output Terminals (VO_OVLO1, 2) are the OR output signals of the chip's built-in over-voltage detection 1 and 2 output signals.
   The flag output logic is shown on the following tables:

Built-In Over-Voltage Detection (OVLO1)	Output (VO_OVLO1)
Non-Detection	Hi-Z
Detection	L

Built-In Over-Voltage Detection (OVLO2)	Output (VO_OVLO2)
Non-Detection	Hi-Z
Detection	L

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4. Self-Check Function

This chip has a built-in self-check function to confirm if its cell balance function is working properly.
When cell balance detection voltage is exceeded, the shunt SW turns ON to make cell balance self-check function possible.
The self-check OK detection output terminal (VO_OK) becomes the AND output of the output signals of the self-check function of each of this LSI's cells. This function is available for 4-, 5- or 6-cell applications.
The plug detection logic is shown on the following table:

Built-In Self-Check Detection	Output (VO_OK)
Non-Detection	Hi-Z
Detection (OK)	L

To cope with 4-cell and 5-cell application, the detection pin gives an output as a dummy when not yet used in the detect block for 5, 6 cells. Because of that, the cell check pin gives output "detect OK (L)" in case the cell 5 or cell 6 is either shorted or damaged. During that time, cell module voltage becomes unbalanced and abnormal detection is possible by monitoring the overvoltage pin "detect (L)" when the cell module becomes fully charged.

5. Detection Time Setting

For cell balance voltage detection (VCB) and over-voltage detection 1, 2 (VOVLO1, 2), the detection time delays can be set for transitions from non-detection to detection and detection to non-detection.
During non-detection, if detection signal matches the 4x td at td=25msec (typ) intervals, the detection flag will output.
Also, during detection, if the non-detection signal matches the 4x td at td=25msec (typ) intervals, the non-detection flag will output.
Through this, detection time delay can be set from 75msec (3x td) to 100msec (4x td) (typ) as detection time delay.

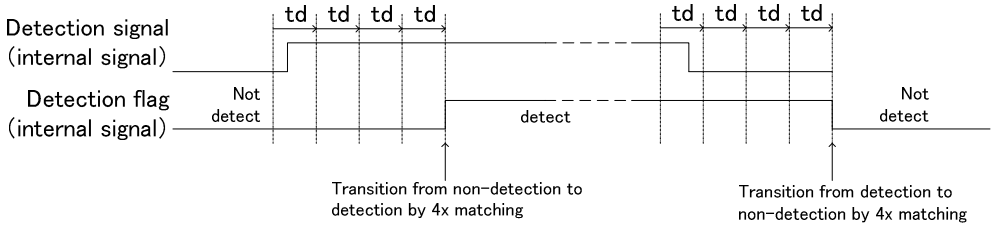


Figure 8. Detection time setting

6. VREG Terminal Application

VREG output voltage is used as I/F power supply and control power supply for the chip's internal blocks.
It is assumed that up to 10mA maximum is applied as external load, and since it is a basic simple power supply, it can only apply power to I/F. Please use only after a thorough inspection of electrical characteristics and confirm that no problem will arise from use.

It is recommended to use a ceramic capacitor with a capacitance equal or greater than 1uF between VREG to VSS.
Please select a capacitor with good DC bias characteristics and with a high capacitance value.

7. Detecting operation when cell voltage is up

Internal detector output of this chip varies with respect to the rise time of the cell voltage. Please use only after a thorough inspection of electrical characteristics and confirm that no problem will arise from use.

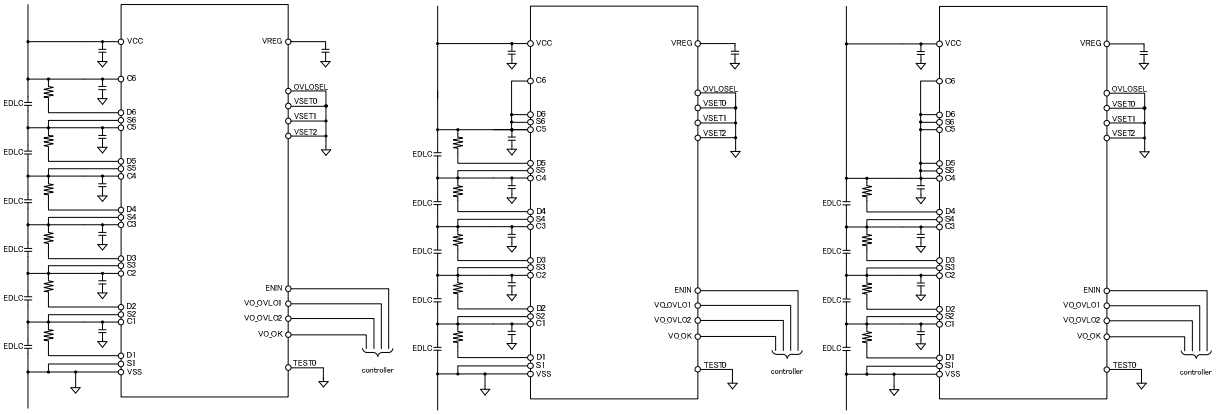
8. Cn(n=1-6) Terminal Application

When detect voltage may be influenced by noise from board or module, please use ceramic capacitors between Cn (n=1-6) to VSS for stable detection only after a thorough inspection of electrical characteristics and confirm that no problem will arise from use.

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Application Example

When using the power storage element with 4 cells and 5 cells, please connect all the unused terminals to the Cn terminal where n is the number of actual cells in series. This chip can respond to 4 to 6 cells, but cannot respond to 3 cells or fewer than 3 cells.



Sample pin connections for 6 cells

Sample pin connections for 5 cells
(Short the unused terminal to C5 terminal)

Sample pin connections for 4 cells
(Short the unused terminals to C4 terminal)

Figure 9. Application circuit

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When using the power storage element for connection of over 8 cells, series connection of this chip is possible. Enable control (ENIN pin control) and flag output (VO_OVLO1, VO_OVLO2, VO_OK pin output) are also available in the series connection by using the following application circuit.

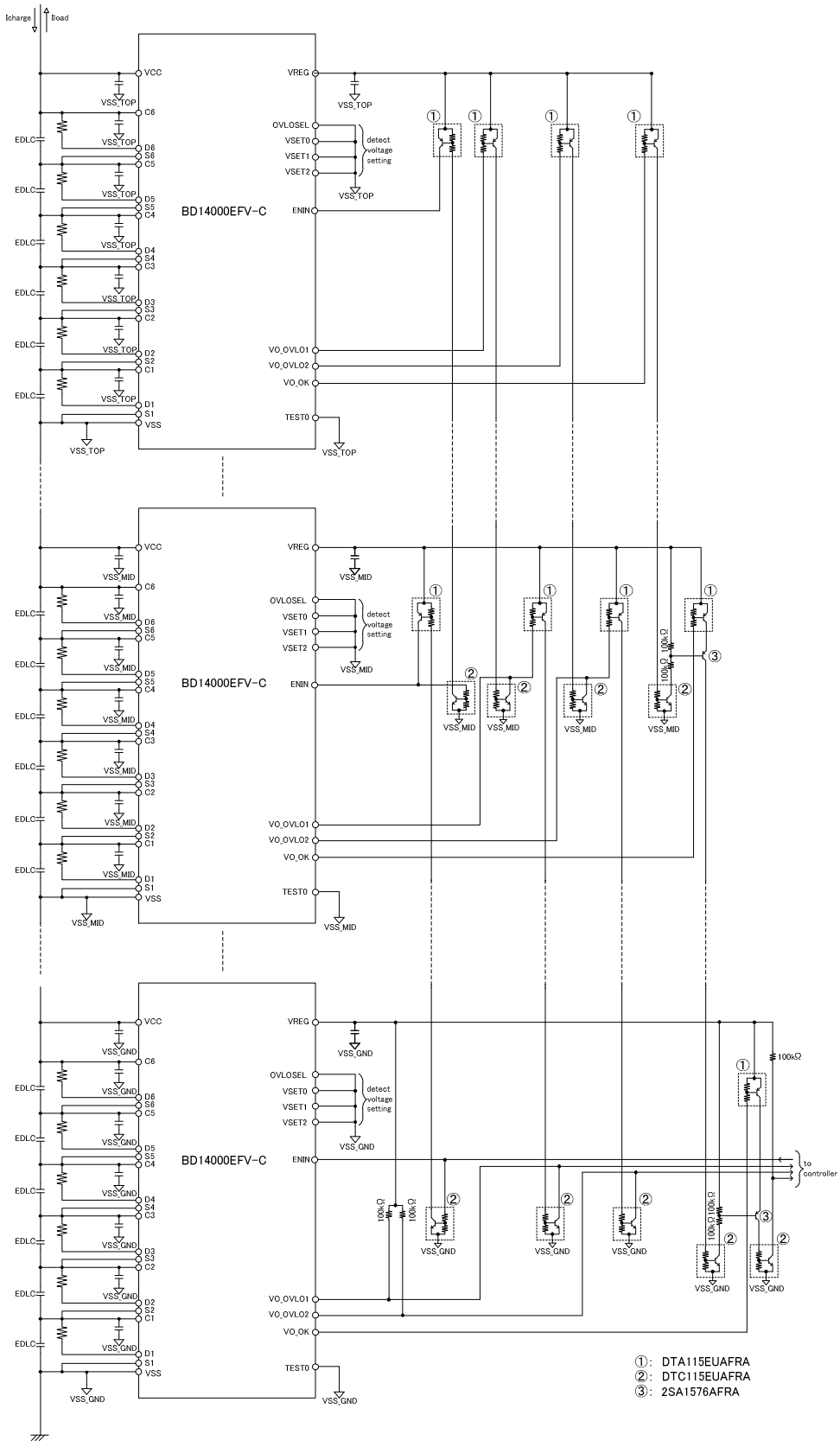


Figure 10. Application circuit for BD14000EFV-C series connection

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Power Dissipation

The maximum allowable junction temperature Tj of BD14000EFV-C is 150°C. Therefore, it is necessary to design the system requirements and the board layout so that the junction temperature does not exceed 150°C in the operating temperature range.

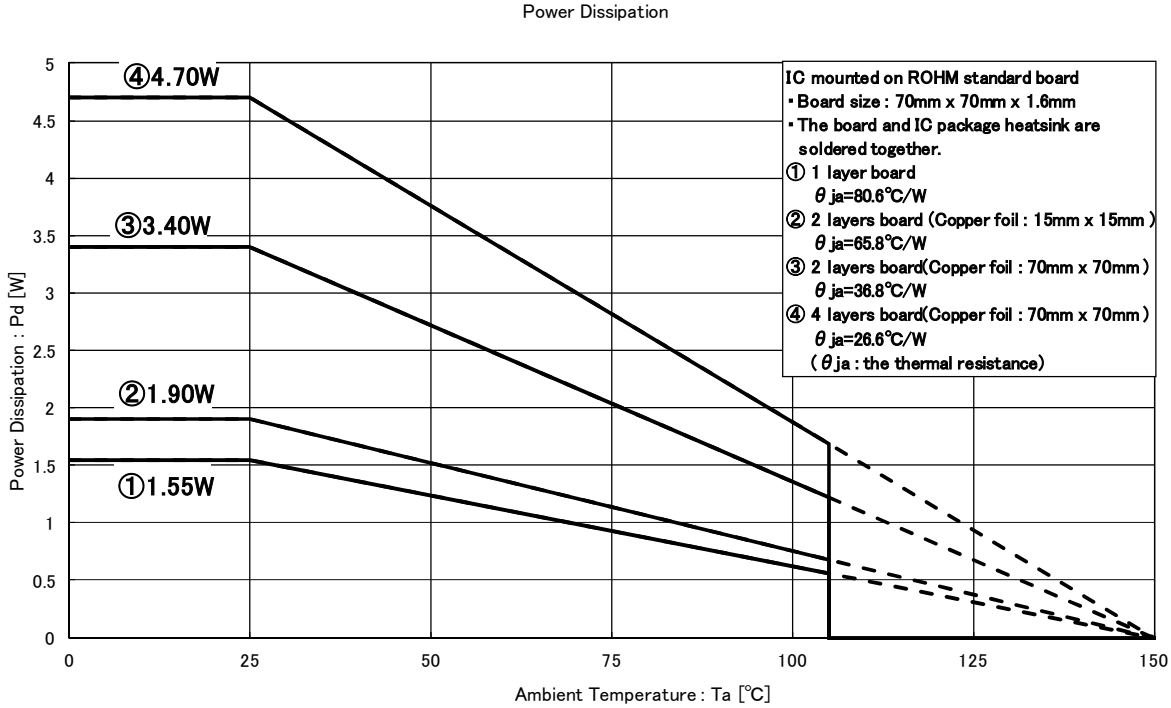


Figure 11. Power Dissipation

[Maximum value of shunt current for cell balance]
Temperature increase, T_{up}[°C], of this chip can be estimated by total power consumption P_{all}[W] and thermal resistance θ_{ja}[°C /W]:

$$T_{up} = P_{all} \times \theta_{ja}$$

Almost all of the power of this chip is consumed by shunt switches:

$$T_{up} = n \times R_{on} \times I_{shunt}^2 \times \theta_{ja}$$

(R_{on}[Ω] = shunt switch on resistance, I_{shunt} [A] = shunt current, n[pcs] = the number of cells)
So, the operating condition is described as follows:

$$T_j - T_{a_max} > T_{up}$$

(T_{a_max}[°C] = maximum operating temperature)
It is possible to decide shunt current value by using this expression.

(Example)
T_j=150°C, T_{a_max}=105°C,
θ_{ja}=80.6°C /W (ROHM standard board, 1 layer board),
R_{on_max}=2.0Ω, n=6pcs

By using the above expressions,

$$150 - 105 > 6 \times 2 \times I_{shunt}^2 \times 80.6$$

$$\Leftrightarrow \quad I_{shunt} < 0.215A$$

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I/O equivalent circuits

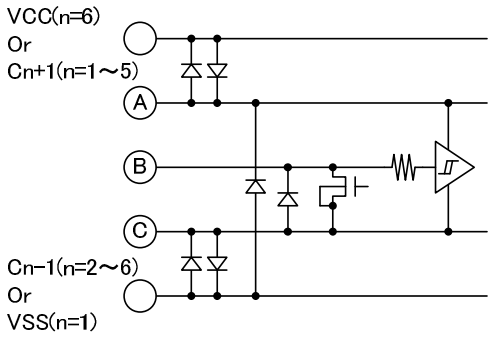
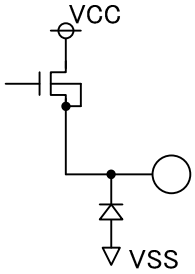
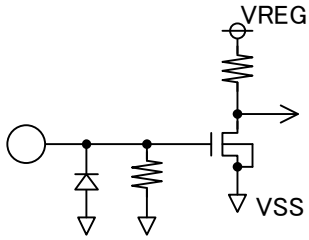
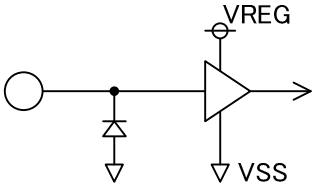
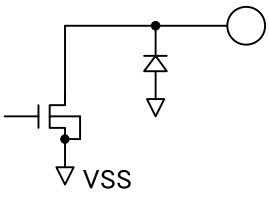
Pin No.	Pin Name	I/O equivalent circuit
1～18	A: Cn B: Dn C: Sn (n=1～6)	
29	VREG	
25 24	ENIN TEST0	
22 21 20 23	VSET0 VSET1 VSET2 OVLOSEL	
28 27 26	VO_OVLO1 VO_OVLO2 VO_OK	

Figure 12. I/O equivalent circuit

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded, the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

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Operational Notes – continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

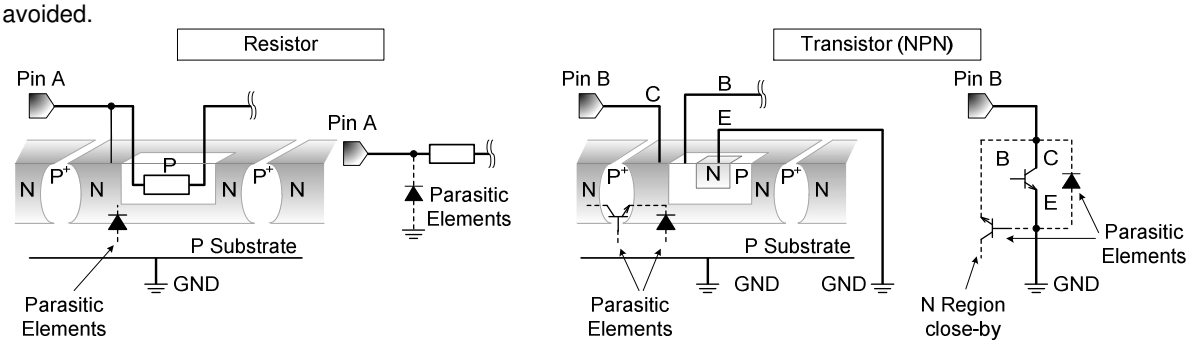


Figure 13. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Over Current Protection Circuit (OCP)

This IC incorporates an integrated over current protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

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Ordering Information

B D 1 4 0 0 0 E F V	-	C E 2

Part Number

Package
EFV: HTSSOP-B30

Product Rank
C: for Automotive
Packaging and forming specification
E2: Embossed tape and reel(2000pcs)

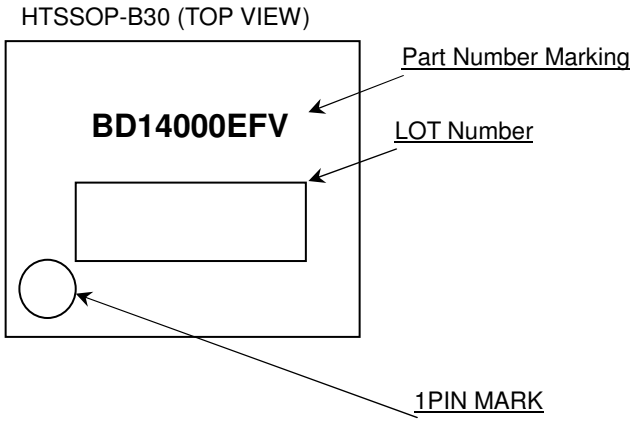
B D 1 4 0 0 0 E F V	-	C H 2

Part Number

Package
EFV: HTSSOP-B30

Product Rank
C: for Automotive
Packaging and forming specification
H2: Embossed tape and reel(250pcs)

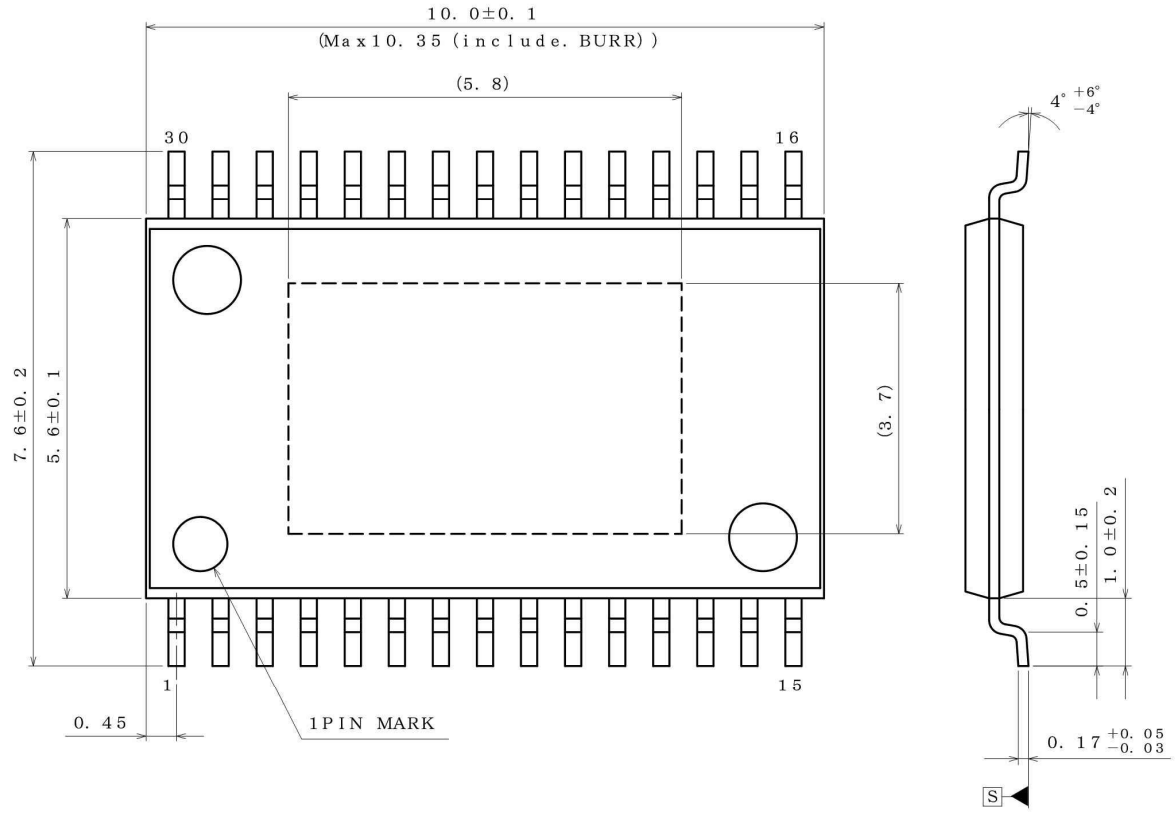
Marking Diagrams



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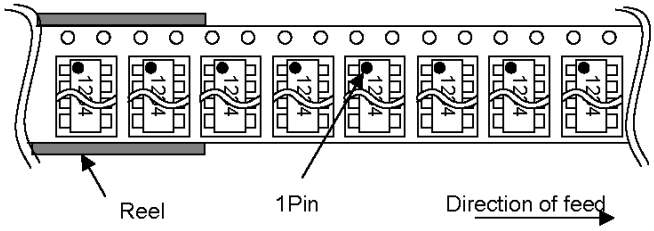
Physical Dimension, Tape and Reel Information

Package Name	HTSSOP-B30



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	E2 : 2000pcs / H2 : 250pcs
Direction of feed	The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



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Revision History

Date	Revision	Changes
9.Jul.2014	001	New Release
22,Jun,2015	002	Added AEC-Q100 operating temperature grade Added Ordering Information for H2 type Added Tape and Reel Information for H2 type

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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